Review Topics for Exam #3

The following is a list of topics that could appear in one form or another on the exam. Not all of these topics will be covered, and it is possible that an exam problem could cover a detail not specifically listed here. However, this list has been made as comprehensive as possible. You should be familiar with the topics on the previous review sheets in addition to those listed below.

Although every effort has been made to ensure that there are no errors in this review sheet, some might nevertheless appear. The textbook is the final authority in all factual matters, unless errors have been specifically identified there. You are ultimately responsible for obtaining accurate information when preparing for your exam.

Schottky barrier diode

“MOSFET” = Metal-Oxide Semiconductor Field Effect Transistor

Internal structure of enhancement-mode MOSFET
- gate is insulated from doped silicon by oxide or polymer layer
- device is usually symmetrical between source and drain (i.e., same geometrical shape and size)
- channel lies inside substrate between source and drain and is usually only microns or a fraction of a micron in length (1 micron = $10^{-6}$ m)
- As of 2013, narrowest channel length in commercially available FETs was 22 nm
- $L =$ channel length (distance from source to drain); $W =$ channel width
- $W/L =$ “aspect ratio”; usually, $W > L$

Qualitative understanding of operation of enhancement-mode MOSFET
- threshold voltage $V_t$
- effect of increasing $v_{GS}$ (charge carriers flood channel as $v_{GS}$ rises above $V_t$)
- effect of increasing $v_{DS}$ (channel bottom tilts as $v_{DS}$ rises to a value comparable to $v_{GS}$)
- directions and polarities of important currents and voltages (e.g., $i_D$ and $v_{DS}$)
- do not confuse drain current $i_D$ in MOSFET with diode current $i_D$ (context)
- depletion region around drain
- formation of channel along substrate directly under gate
- pinchoff condition present when FET is in saturation (constant-current) region; current still flows, but it does not continue to increase much with increasing $v_{DS}$
- electron and hole mobilities; typical values for doped silicon are $\mu_n = 480$ cm$^2$/V·s and $\mu_p = 190$ cm$^2$/V·s; $\mu_n$ is approximately 2.5 times $\mu_p$
- capacitance of gate per unit area, $C_{ox} = \varepsilon_{ox} / t_{ox}$ ($\varepsilon_{ox}$, $t_{ox}$ = permittivity and thickness of oxide layer); typical values are around 1-10 fF/µm$^2$
- process transconductance parameter $k'_n = \mu_n C_{ox}$ or $k'_p = \mu_p C_{ox}$; unit is A/V$^2$
- MOSFET transconductance parameter (includes aspect ratio $W/L$):

$$k_n = \mu_n C_{ox} \frac{W}{L} = k'_n \frac{W}{L} \quad \text{and} \quad k_p = \mu_p C_{ox} \frac{W}{L} = k'_p \frac{W}{L}$$
- $\mu_n$ ($\mu_p$) and $V_t$ are highly temperature dependent, but $\mu_n$ ($\mu_p$) usually dominates
MOSFET $i$-$v$ characteristic for $v_{DS} \ll v_{GS}$ ($i_D$ vs. $v_{DS}$ for selected values of $v_{GS}$)

- **cut-off region**
  - $v_{GS} < V_t$
  - $i_D = 0$

- **triode region**
  - $v_{GS} < V_t$ and $v_{DS} < v_{GS} - V_t$
  - Drain current expression for NMOS (similar for PMOS):
    \[
    i_D = k_n \left( (v_{GS} - V_t) v_{DS} - \frac{1}{2} v_{DS}^2 \right)
    \]
  - if $v_{DS} \ll v_{GS}$, MOSFET acts as voltage-controlled resistor (similar expression for PMOS):
    \[
    i_D \approx k_n (v_{GS} - V_t) v_{DS} \quad \rightarrow \quad \frac{v_{DS}}{i_D} = r_{DS} = \frac{1}{k_n (v_{GS} - V_t)}
    \]

- **saturation region**
  - $v_{GS} < V_t$ and $v_{DS} \geq v_{GS} - V_t$
  - Drain current expression for NMOS (similar for PMOS):
    \[
    i_D = \frac{1}{2} k_n (v_{GS} - V_t)^2
    \]

$n$-channel vs. $p$-channel MOSFETs (NMOS and PMOS)
- comparison of electron mobility $\mu_n$ vs. hole mobility $\mu_p$ (hole mobility is approximately 0.4 times electron mobility for doped Si)
- $v_{GS}$, $v_{DS}$, and $V_t$ are all negative for enhancement-mode PMOS
- $i_D$ is positive for both types (Sedra and Smith’s convention)
- $i$-$v$ characteristics of NMOS and PMOS have voltages of opposite sign

MOSFET circuit symbols
- $n$-channel vs. $p$-channel
- simpler symbol when substrate is tied to source internally
- pay attention to directions of arrows

MOSFET substrates
- NMOS substrate (which is made of $p$-type material) must be connected to most negative voltage in circuit to avoid forward-biasing the pn junctions
- PMOS substrate (which is made of $n$-type material) must be connected to most positive voltage in circuit to avoid forward-biasing the pn junctions

CMOS digital logic gates
- use no resistors
- negligible drain current once equilibrium is established after logical state change
- MOSFETs are either in cutoff (“off”) or triode region ($v_{DS} \approx 0$ because $i_D \approx 0$) in all logical states

General analysis techniques for MOSFET circuits
- determination of region of operation (cutoff, saturation, or triode)
- $v_{DS}$ for $n$-channel MOSFETs is typically zero or positive (negative for PMOS)
- graphical analysis techniques (load lines) can be applied
- resolution of sign ambiguities when quadratic formula is required due to square-law dependence of $i_D$ on $v_{GS}$

MOSFET attenuator circuits
- assumes $v_{DS} \ll v_{GS} - V_t$, thus operation in triode region
- channel under gate has almost constant depth along length
- no DC quiescent current through drain-to-source path ($i_D = 0$, but $i_d \neq 0$)
- no DC quiescent drain-to-source voltage \( (V_{DS} = 0, \text{ but } v_{ds} \neq 0) \)
- acts as a voltage controlled resistor for small signals:
  \[
  r_{DS} = \frac{1}{k_n (V_{GS} - V_t)}, \quad \text{(NMOS)} \quad \text{where } V_{GS} \text{ is the quiescent gate-to-source voltage}
  \]
- nonlinear if \( v_{ds} \) becomes too large; can "linearize" attenuator by adding a large resistance between drain and gate and another large resistance of equal value between gate and DC control voltage source so that \( v_{gs} = 0.5 v_{ds} \) (small-signal voltage relationship):
  \[
  i_D = k_n \left[ (v_{GS} - V_t) v_{DS} - \frac{1}{2} v_{DS}^2 \right] = k_n \left[ (V_{GS} + v_{gs} - V_t) v_{DS} - \frac{1}{2} v_{ds}^2 \right] = k_n \left( V_{GS} - V_t \right) v_{ds}
  \]
  where \( v_{GS} = V_{GS} + v_{gs} \) (quiescent + small-signal) and \( v_{DS} = v_{ds} \) (quiescent drain-to-source voltage is zero in an attenuator)

MOSFETs in “diode-connected transistor” configuration
- useful for biasing on IC MOSFET circuits without using resistors
- gate tied to drain, so \( V_{GS} = V_{DS} \)
- FET is almost always in saturation region, never in triode region (could be cut off)
  - \( i_D = \frac{1}{2} k_n (v - V_t)^2 \), where \( v \) is the voltage across the MOSFET \( (v = v_{GS} = v_{DS}) \)
  - PMOS devices can also be configured this way; \( i-v \) characteristic is
    \[
    i_D = \frac{1}{2} k_p (v_{GS} - V_t)^2 \quad \text{or} \quad i_D = \frac{1}{2} k_p (|v_{gs}|)^2
    \]
    because \( v_{GS} \) is negative

Distinction between bias, signal, and total voltages and currents
- signals are usually time-varying, but don’t have to be
- signals contain information (audio, video, data, sensor outputs, etc.)
- bias conditions (DC levels) define the “Q-point” (quiescent point)
- total voltage or current is sum of bias and signal components (superposition)
- conventions:
  - lower-case variable w/upper-case subscript: total (DC + signal) quantity
  - upper-case variable w/upper-case subscript: quiescent DC quantity
  - lower-case variable w/lower-case subscript: signal (AC) quantity

Biasing MOSFET circuits
- concept of biasing and why it is necessary
- the parameters \( k_n \) (\( k_p \)) and \( V_t \) have strong temperature dependence and device variation
- design for quiescent output voltage, drain current, and/or voltage drop across source resistor
- usually bias MOSFET for operation in the saturation region if it’s used as amplifier
- must pay attention to swing range of \( v_D \) to avoid cutoff and triode regions
  - in cutoff region, \( i_D = 0 \); this is also true at the boundary between the cutoff and saturation regions
  - saturation-triode boundary defined by (for NMOS devices):
    \[
    V_D \bigg|_{\text{sat--triode}} = V_G - V_t \quad \text{or} \quad V_{DS} \bigg|_{\text{sat--triode}} = V_{GS} - V_t
    \]
parameter-independent biasing (source degeneration), or “4-resistor” biasing
  - must satisfy $I_D = 0.5k_n(V_{GS} - V_t)^2$ and $V_{GS} = V_G - I_D R_S$ simultaneously
  - square-law relationship sometimes leads to solution of quadratic equations
  - must determine which solution to quadratic equation is the physical solution
  - exact solution: $I_D = \frac{V_G - V_t}{R_S} + \frac{1}{k_n R_S^2} - \frac{1}{k_n R_S^2} \sqrt{1 + 2k_n R_S(V_G - V_t)}$
  - design rules of thumb: $I_D R_D = I_D R_S = \frac{1}{3} V_{DD}$ and $V_G = I_D R_S + V_t + \sqrt{2I_D / k_n}$, but $V_D$ value could be explicitly specified, which
    could mean $I_D R_D \neq \frac{1}{3} V_{DD}$
  - establishment of gate bias voltage simplified because $I_G = 0$
    - $V_G = V_{DD} \frac{R_B}{R_A + R_B}$, if $R_B$ is the “lower” resistor (between gate and ground)
  - biasing using a drain-to-gate feedback resistor, including variant with gate-to-ground resistor
  - gate biasing resistors should be in the MΩ range or several 100s of kΩ to avoid
    loading down signal source applied to amplifier’s input

DC blocking capacitors
  - act as open circuits at DC
  - act as short circuits (or have sufficiently low reactance) at signal frequencies
  - isolate DC biasing from effects of source and/or load

General small-signal modeling
  - definition of “incremental signal” or “small signal” (fluctuations are a small fraction
    of bias level)
  - separation of bias considerations (quiescent levels; output voltage swing range) from
    small-signal considerations (gain, input and output resistance)
  - for small-signal (AC) analysis,
    - replace DC voltage sources with short circuits (because voltage across a DC
      voltage source can’t change)
    - replace DC current sources with open circuits (because current through a DC
      current source can’t change)
    - replace large capacitors with short circuits (if capacitive reactance is
      insignificant at operating frequency)
    - replace of large inductors with open circuits (if inductive reactance is very
      large at operating frequency)
  - DC voltage sources are typically bypassed at AC (i.e., at signal frequency) using
    capacitors to ensure that the source acts as an AC ground.
  - small-signal model of MOSFET comprised of $g_m$ and $r_o$ is only valid when device
    operates in the saturation region
  - small-signal model of drain-to-source path represented by $r_{DS}$ is only valid when
    MOSFET operates in the low-$v_{DS}$ triode region
  - small-signal model of MOSFET in cut-off region consists of open circuits between all
    terminals (gate, source, drain)
  - derivation of small-signal voltage gain $v_o/v_{in}$ or $(v_o/v_{sig})$
  - simplifications can sometimes be made in gain expressions when one term is much
    greater/smaller than another term
Small-signal modeling of MOSFET amplifier circuits
- gate-source path modeled as an open circuit
- small-signal transconductance $g_m$
  - basic definition: $g_m = \frac{\partial i_D}{\partial v_{gs}} \bigg|_{v_{gs}=V_{gs}}$; can also be derived from
  $$I_D + i_d = \frac{1}{2} k_n (V_{GS} + V_{gs} - V_t)^2 = \frac{1}{2} k_n (V_{GS} - V_t)^2 + k_n (V_{GS} - V_t) v_{gs} + \frac{1}{2} k_n v_{gs}^2$$
  $$\approx \frac{1}{2} k_n (V_{GS} - V_t)^2 + k_n (V_{GS} - V_t) v_{gs}$$
  $$\rightarrow i_d = k_n (V_{GS} - V_t) v_{gs} = g_m v_{gs},$$
  where $|v_{gs}| << 2(V_{GS} - V_t)$ and $g_m = k_n(V_{GS} - V_t)$
  - equivalent formulas (these are for NMOS devices; similar for PMOS):
    $$g_m = k_n V_{ov} = k_n (V_{GS} - V_t) = \frac{2I_D}{V_{GS} - V_t} = \sqrt{2k_n I_D},$$
    where $k_n = k'_n W/L = \mu_n C_{ox} W/L$
    - derivations of these formulas
- effect of source degeneration resistor ($R_S$) on gain
- incremental drain-source resistance $r_o$
  - represents non-zero slope of $i_D$-v$_{DS}$ characteristic in the saturation region due to channel-length modulation (sometimes referred to as the Early effect, although that term technically applies only to BJTs)
  - i-v characteristic in saturation region that includes $\lambda$:
    $$i_D = \frac{1}{2} k_n v_{ov}^2 [1 + \lambda (v_{DS} - v_{ov})] \approx \frac{1}{2} k_n v_{ov}^2 (1 + \lambda v_{DS}),$$
    where $v_{ov} = V_{GS} - V_t$
  - channel-length modulation parameter: $\lambda = \frac{1}{V_A + V_{ov}} \approx \frac{1}{V_A}$,
    where $V_A = $ Early voltage
  - $r_o$ is typically 20-100 k$\Omega$ for MOSFETs but can be much lower for some types
  - $r_o$ is not equal to $r_{DS}$ of MOSFET in low-v$_{DS}$ triode region!
  - $r_o \approx \frac{V_A}{I_D} \approx \frac{1}{\lambda I_D}$

Common-source (CS) and common-drain (source follower) amplifiers

Relevant course material:

HW: #6 and #7
Labs: #8 through #10
Textbook: Sec. 4.7.1, Secs. 5.1, 5.2, 5.3, 5.4, 5.5.1-5.5.6, 5.6.1-5.6.3, 5.6.6, 5.7, 5.9.1-5.9.3
Lecture notes: “Source Degeneration Biasing for Discrete MOSFET Amplifiers”
Web Links: (none)
Mathcad: (none)
Matlab: (none)