Final Exam General Information

Rough breakdown of topic coverage:

- 10-25% BJT fundamentals and regions of operation
- 20-40% MOSFET fundamentals, biasing, and small-signal modeling
- 10-15% Diodes (pn-junction diodes, zener diodes)
- 0-15% Basic difference amplifiers, instrumentation amplifiers, and CMRR
- 0-15% DC imperfections in op amps (input bias current, input offset voltage)

See the “Course Outcomes” section of the Course Description page at the ELEC 350 web site for a more detailed list of specific competencies that are likely to be assessed.

The final exam will take place **3:30-6:30 pm on Tuesday, December 16 in Breakiron 166 [day of week and location corrected 12/13/2014]**. The exam will be designed to be approximately 1.5 hours in length, but you will have the full three hours to complete it.

You will be allowed to use up to four 8.5 x 11-inch two-sided help sheets and a non-wireless enabled calculator, such as a TI-99. There are no restrictions on the material you may place on the help sheets except that they must be entirely handwritten. Please note that **all help sheets will be collected at the end of the exam** but will be returned to you later if you wish to have them back.

The final exam score cannot be dropped. Solutions to the final exam will not be posted, but you may review your final exam and discuss it with me after it has been graded.

### Review Topics for Final Exam

The following is a list of topics that could appear in one form or another on the exam. Not all of these topics will be covered, and it is possible that an exam problem could cover a detail not specifically listed here. However, this list has been made as comprehensive as possible. You should be familiar with the topics on the previous review sheets in addition to those listed below.

Although every effort has been made to ensure that there are no errors in this review sheet, some might nevertheless appear. The textbook is the final authority in all factual matters, unless errors have been specifically identified there either by the authors (in the form of published errata) or by me. You are ultimately responsible for obtaining accurate and authoritative information when preparing for your exam.

**Determination of MOSFET region of operation**

- try to determine gate voltage, if possible; helps to rule out (or not) cut-off region
- assume MOSFET is in one region and analyze the circuit based on that assumption
- check all voltages and currents and determine whether or not their values are consistent with the initial assumption. If so, analysis is complete. If not, use the results of the initial analysis to determine likely region of operation. Repeat analysis under new assumption and confirm.
Biasing MOSFET circuits
- concept of biasing and why it is necessary
- parameters $k_n$, $k_p$, and $|V_t|$ decrease with increasing temperature (strong dependence)
- design for quiescent output voltage, drain current, and/or voltage drop across source resistor
- usually bias MOSFET for operation in the saturation region if it’s used as amplifier
- must pay attention to swing range of $v_D$ to avoid cutoff and triode regions
  - in cutoff region, $i_D = 0$; this is also true at the boundary between the cutoff and saturation regions
  - saturation-triode boundary defined by (for NMOS devices): $V_D|_{\text{sat-triode}} = V_G - V_t$ or (equivalently) $V_{DS|\text{sat-triode}} = V_{GS} - V_t$
- parameter-independent biasing (source degeneration), or “4-resistor” biasing

\[
V_G = I_D R_S + V_t + \sqrt{2I_D R_S / k_n},
\]
but $V_D$ value could be explicitly specified, which could mean $I_D R_D = \frac{1}{3} V_{DD}$.

- establishment of gate bias voltage simplified because $I_G = 0$:

\[
V_G = V_{DD} \frac{R_B}{R_A + R_B},
\]
where $R_B$ is the “lower” resistor (b/w gate and ground)
- biasing using a drain-to-gate feedback resistor, including variant with gate-to-ground resistor
- gate biasing resistors should be in the MΩ range or several 100s of kΩ to avoid excessive current draw from power supply and to avoid loading down signal source applied to amplifier’s input

DC blocking capacitors
- act as open circuits at DC
- act as short circuits (or have sufficiently low reactance) at signal frequencies
- isolate DC biasing from effects of signal source and/or load
General small-signal modeling
- definition of “incremental signal” or “small signal” (fluctuations are a small fraction of bias level)
- separation of bias considerations (quiescent levels; output voltage swing range) from small-signal considerations (gain, input and output resistance)
- for small-signal (AC) analysis,
  o replace DC voltage sources with short circuits (because voltage across a DC voltage source can’t change; alternative reason: a 0-V source is a short)
  o replace DC current sources with open circuits (because current through a DC current source can’t change; alternative reason: a 0-A source is an open)
  o replace large capacitors with short circuits (if capacitive reactance is insignificant at operating frequency)
  o replace small capacitors with open circuits (if capacitive reactance is enormous at operating frequency)
  o replace large inductors with open circuits (if inductive reactance is very large at operating frequency)
  o replace small inductors with short circuits (if inductive reactance is insignificant at operating frequency)
- DC voltage sources are typically bypassed at AC (i.e., at signal frequency) using large capacitors to ensure that the source acts as an AC ground.
- small-signal model of MOSFET comprised of $g_m$ and $r_o$ is only valid when device operates in the saturation region
- small-signal model of drain-to-source path represented by $r_{DS}$ is only valid when MOSFET operates in the low-$V_{DS}$ triode region
- small-signal model of MOSFET in cut-off region consists of open circuits between all terminals (gate, source, drain)
- derivation of small-signal voltage gain $v_o/v_{in}$ or $(v_o/v_{sig})$
- simplifications can sometimes be made in gain expressions when one term is much greater/smaller than another term

Small-signal modeling of MOSFET amplifier circuits
- gate-source path modeled as an open circuit
- small-signal transconductance $g_m$
  o basic definition: $g_m = \frac{\partial i_D}{\partial v_{GS}} \bigg|_{v_{GS} = V_{GS}}$; can also be derived from

$$I_D + i_d = \frac{1}{2} k_n (V_{GS} + v_{gs} - V_t)^2 = \frac{1}{2} k_n (V_{GS} - V_t)^2 + k_n (V_{GS} - V_t) v_{gs} + \frac{1}{2} k_n v_{gs}^2$$

$$\approx \frac{1}{2} k_n (V_{GS} - V_t)^2 + k_n (V_{GS} - V_t) v_{gs}$$

$$\rightarrow i_d = k_n (V_{GS} - V_t) v_{gs} = g_m v_{gs},$$

where $|v_{gs}| << 2(V_{GS} - V_t)$ and $g_m = k_n(V_{GS} - V_t)$
  o equivalent formulas (these are for NMOS devices; similar for PMOS):

$$g_m = k_n V_{OV} = k_n (V_{GS} - V_t) = \frac{2I_p}{V_{GS} - V_t} = \sqrt{2}\frac{k_n I_D}{V_{GS} - V_t},$$

where $k_n = k_n' \frac{W}{L} = \mu_n C_{ox} \frac{W}{L}$
  o derivations of these formulas
- effect of source degeneration resistor ($R_s$) on gain
- incremental drain-source resistance \( r_o \)
  - represents non-zero slope of \( i_D-v_{DS} \) characteristic in the saturation region due to channel-length modulation (sometimes referred to as the Early effect, although that term technically applies only to BJTs)
  - \( i-v \) characteristic in saturation region that includes \( \lambda \):
    \[
    i_D = \frac{1}{2} k_n v_{OV}^2 \left[ 1 + \lambda (v_{DS} - v_{OV}) \right] \approx \frac{1}{2} k_n v_{OV}^2 \left( 1 + \lambda v_{DS} \right),
    \]
    where \( v_{OV} = v_{GS} - V_t \)
  - channel-length modulation parameter:
    \[
    \lambda = \frac{1}{V_A + V_{OV}} \approx \frac{1}{V_A},
    \]
    where \( V_A = \text{Early voltage} \)
  - \( r_o \) is typically 20-100 k\( \Omega \) for MOSFETs but can be much lower for some types
  - \( r_o \) is not equal to \( r_{DS} \) of MOSFET in low-\( v_{DS} \) triode region!
  - \( r_o \approx \frac{V_A}{I_D} \approx \frac{1}{\lambda I_D} \)

Common-source (CS) and common-drain (source follower) amplifiers
- “common” refers to terminal connected either directly to ground or to ground through a few resistors, capacitor, and maybe inductors. Signal source and load are connected to other terminals (directly or indirectly) not indicated as “common.”
- CS amps and source followers can be biased in multiple ways; i.e., the biasing network does not determine the amplifier’s nomenclature

Internal structure of bipolar junction transistor (BJT)
- \( npn \): thin \( p \)-type base sandwiched between \( n \)-type emitter and collector
- \( pnp \): opposite of \( npn \)
- base-emitter (BE) and collector-base (CB) junctions are regular \( pn \) junctions and act the same way (i.e., they can be forward or reverse-biased; they have turn-on voltages)
- BJTs can be modeled as back-to-back diodes (base is the node b/w diodes)

BJT circuit symbols
- pay attention to directions of arrows (arrow indicates the emitter terminal and BJT type; arrow of \( npn \) is “not pointing in”)

\[
\text{npn} \quad \begin{array}{c}
B \\
C \\
E
\end{array} \quad \text{pnp} \quad \begin{array}{c}
B \\
C \\
E
\end{array}
\]

\text{npn vs. pnp} BJTs
- \( v_{BE} \) and \( v_{CE} \) of \( npn \) BJTs have positive values in normal operation
- \( v_{BE} \) and \( v_{CE} \) of \( pnp \) BJTs have negative values in normal operation (use \( v_{EB} \) and \( v_{EC} \), which are positive, instead)
- \( i_B \) and \( i_C \) flow into base and collector terminals of \( npn \) BJTs and out of base and collector terminals of \( pnp \) BJTs
- \( i-v \) characteristics of \( npn \) and \( pnp \) BJTs have voltages of opposite sign

Qualitative understanding of operation of BJT
- turn-on voltage (\( V_F \)) of base-emitter junction (approx. 0.7 V for Si)
- effect of changing base current \( i_B \)
- effect of changing collector-emitter voltage \( v_{CE} \) (normally CB junction is reverse biased or at least not heavily forward biased; necessary for collector current to flow)
- directions and polarities of important currents and voltages (\( i_B, i_C, i_E, v_{BE}, v_{CE} \))
- thin base region required to allow electrons (\textit{nnp}) or holes (\textit{pnp}) to flow from emitter to collector
- emitter more heavily doped than base – allows base to fill with minority carriers (electrons for \textit{nnp}; holes for \textit{pnp}) when base current flows
- base-emitter junction is forward biased if $v_{BE}$ is at turn-on voltage ($V_F$)
- \textit{i-v} characteristic of BE junction is the same as that of a \textit{pn}-junction diode:
  \[ i_B = I_{SB}e^{v_{BE}/nV_T}, \]
  where $I_{SB}$ = saturation current of BE junction, $n$ = emission coefficient (typically assumed to equal one), and $V_T$ = thermal voltage, which is given by
  \[ V_T = \frac{T}{11,600}, \]
  where $T$ = temperature in kelvins ($V_T = 25$ mV at room temp.)
- collector-base junction is usually reverse biased (produces depletion region) or lightly forward biased
- collector current related to base current by $i_C = \beta i_B$ in the active region, where $\beta$ = forward DC current gain (values are typically 20-300, but vary among BJT types, even among individual units of a given type within the same manufacturing batch; $\beta$ varies strongly with temperature)

\textbf{BJT \textit{i-v} characteristic ($i_C$ vs. $v_{CE}$ for selected values of $i_B$)}
- cut-off region ($v_{BE} < V_F$, where $V_F$ = turn-on voltage of BE junction; $i_B = i_C = 0$)
- active (constant-current) region ($v_{BE} = V_F$, $i_C = \beta i_B$, $v_{CE} > 0.2-0.3$ V)
- saturation region ($v_{BE} = V_F$, $v_{CE} \approx 0.2-0.3$ V, and $i_C < \beta i_B$, but $i_C$ is nonzero)

\textbf{General analysis techniques for BJT circuits}
- determination of region of operation (cutoff, active, or saturation)
  o try to determine if base-emitter junction is forward biased, if possible; helps to rule out (or not) cut-off region
  o assume BJT is in one region and analyze the circuit based on that assumption
  o check all voltages and currents and determine whether or not their values are consistent with the initial assumption. If so, analysis is complete. If not, use the results of the initial analysis to determine likely region of operation.
  Repeat analysis under new assumption and confirm.
- $v_{CE}$ (for \textit{nnp} BJT) is always positive (negative for \textit{pnp}; i.e., $v_{EC}$ is positive)
- $v_{BE} \approx 0.7$ V (for Si \textit{nnp}) in the active and saturation regions
- in cut-off region, $i_B = i_C = 0$ and $v_{BE} < 0.7$ V (for Si \textit{pnp})
- in active region, $v_{BE} \approx 0.7$ V, $i_C = \beta i_B$ and $v_{CE} > v_{CE|sat} \approx 0.2-0.3$ V
- in saturation region, $v_{BE} \approx 0.7$ V, $i_C < \beta i_B$ and $v_{CE} = v_{CE|sat} \approx 0.2-0.3$ V
- for more accurate analysis (rarely necessary), use
  \[ i_B = I_{SB}e^{v_{BE}/nV_T}, \]
  where $I_S$ = saturation current, $n$ = emission coefficient (typically assumed to equal one), and $V_T$ = thermal voltage

\textbf{BJT inverter circuits}
- can be used as logical NOT gates
- transfer characteristic ($v_o$ vs. $v_{in}$) has negative slope in active region and nearly zero slope in cut-off and saturation regions
- BJT inverter is also called a common-emitter amplifier
- has an almost linear transfer characteristic in active region
Four-resistor BJT biasing circuit

- for analysis purposes, can represent base biasing network by a Thévenin equivalent circuit consisting of: $V_{BB} = V_{CC} \frac{R_2}{R_1 + R_2}$ and $R_{BB} = R_1 \parallel R_2$;

simplifies evaluation of $I_B$
- design for quiescent output voltage, collector current, and/or voltage drop across emitter resistor (if present)
- usually bias BJT for operation in the active region
- the parameter $\beta$ has strong temperature dependence and device variation
- negative feedback via emitter degeneration resistor stabilizes $I_C$
- current through $R_1$ and $R_2$ is typically designed to be 0.1 to 1 times $I_E$ (or 10-100 times $I_B$)
- resistors $R_1$ and $R_2$ do not behave as a true voltage divider because $I_B \neq 0$; however, they approximate a voltage divider because $I_B$ should be small compared to current through $R_1$ and $R_2$ (1/10 or less)
- trade-off: higher current through $R_1$ and $R_2$ leads to more stable quiescent point but lower input resistance and higher current demand from power supply
- common design rule of thumb: $I_C R_C = I_E R_E = \frac{1}{3} V_{CC}$, although the voltage across $R_E$ is sometimes designed to be less than this (if $V_B$ set to $V_{CC}/3$)
- variation for bipolar (pos./neg.) power supplies: use $R_E$ and $R_C$ but only a single resistor ($R_B$) from base to ground

Relevant course material:

HW: #8
Labs: #6
Textbook: Sections 5.2.4, 5.2.5, 5.4.1-5.4.6, 5.5.1-5.5.6, 5.6.1-5.6.3, 5.6.6, 5.7.1-5.7.3, 5.8.1-5.8.2, 5.8.5, 6.1, 6.2, 6.3, 6.7.1-6.7.2
Lecture notes: “Source Degeneration Biasing for Discrete MOSFET Amplifiers”
Web Links: (none)
Mathcad: (none)
Matlab: (none)