Introduction

Biasing is the process of selecting component values in an amplifier so that the proper quiescent voltages and currents in the circuit are established to meet a set of design goals. A frequent requirement is to have the quiescent voltages and currents remain close to target values in spite of variations in device parameters. In other situations the repeatability of specific voltage and current levels is not so important, but their stability in spite of temperature changes or other environmental variations is important. In this lab exercise you will design and test a bias circuit for a 2N7000 n-channel enhancement-mode MOSFET.

Pre-Lab Work and Quiz

There will be no quiz or pre-lab work for this lab exercise, except to read over this handout carefully before the lab session. The more familiar you are with the task ahead, the more efficiently you will be able to use your lab time.

Theoretical Background

Bias levels in MOSFET amplifiers are often stabilized using the source degeneration technique, in which a resistor is placed between the device’s source and ground. The resistor introduces negative feedback that forces the quiescent drain current to remain close to its design value regardless of changes in the MOSFET’s parameters ($k_n$ or $k_p$, and $V_t$). Figure 1 shows a common-source amplifier that uses this bias stabilization method. If the drain current $I_D$ begins to rise above its intended quiescent value, the voltage drop across $R_S$ increases. Since the gate-source voltage $V_{GS}$ is the difference between the gate potential $V_G$ and the voltage across $R_S$, a rise in the latter causes $V_{GS}$ to drop, which in turn causes $I_D$ to move back toward its original value. Gate voltage $V_G$ is very stable because it is established by the voltage divider formed by $R_A$ and $R_B$. The opposite chain of events occurs if $I_D$ begins to drop below its intended value.

![Figure 1. Common-source amplifier using an n-channel enhancement-mode MOSFET with source degeneration. The dashed lines indicate that the capacitors, the source $v_{gs}$, and the load $R_L$ do not affect the DC biasing of the circuit.](image)
The quiescent drain current $I_D$ in an amplifier with source degeneration must simultaneously satisfy the two relationships

$$I_D = \frac{1}{2} k_n (V_{GS} - V_t)^2 \quad \text{and} \quad V_{GS} = V_G - I_D R_S,$$

where $V_t$ is the threshold voltage of the MOSFET, and $k_n$ is its transconductance parameter, which is given by

$$k_n = \mu_n C_{ox} \frac{W}{L},$$

where $\mu_n$ is the mobility of the free electrons in the inversion channel, $C_{ox}$ is the capacitance per unit area between the gate and the channel, and $W$ and $L$ are the width and length, respectively, of the channel. The quantity $V_G$ is the gate voltage measured with respect to ground. Combining the two $I_D$-$V_{GS}$ equations by eliminating $V_{GS}$ leads to a quadratic equation:

$$I_D = \frac{1}{2} k_n (V_G - I_D R_S - V_t)^2 = \frac{1}{2} k_n [(V_G - V_t) - I_D R_S]^2$$

$$= \frac{1}{2} k_n [(V_G - V_t)^2 - 2(V_G - V_t) I_D R_S + I_D^2 R_S^2]$$

$$\rightarrow \frac{2I_D}{k_n} = (V_G - V_t)^2 - 2(V_G - V_t) I_D R_S + I_D^2 R_S^2$$

$$\rightarrow R_S^2 I_D^2 - \left[2R_S (V_G - V_t) + \frac{2}{k_n}\right] I_D + (V_G - V_t)^2 = 0.$$

The solution is

$$I_D = \frac{2R_S (V_G - V_t) + 2/k_n}{2R_S^2} \pm \frac{1}{2R_S^2} \sqrt{4R_S^2 (V_G - V_t)^2 + 8 R_S (V_G - V_t) + 4}$$

$$= \frac{V_G - V_t}{R_S} + \frac{1}{k_n R_S^2} \pm \frac{1}{2R_S^2} \sqrt{4R_S^2 (V_G - V_t)^2 + 8 R_S (V_G - V_t) + 4}$$

$$= \frac{V_G - V_t}{R_S} + \frac{1}{k_n R_S^2} \pm \frac{1}{2R_S^2} \sqrt{\frac{4}{k_n^2} [2k_n R_S (V_G - V_t) + 1]}$$

$$= \frac{V_G - V_t}{R_S} + \frac{1}{k_n R_S^2} \pm \frac{1}{k_n^2 R_S^2} \sqrt{1 + 2k_n R_S (V_G - V_t)}$$

The sign ambiguity is resolved by applying the constraint $V_{GS} > V_t$. Since $V_{GS} = V_G - I_D R_S$, then

$$V_{GS} > V_t \rightarrow V_G - I_D R_S > V_t \rightarrow V_G - V_t > I_D R_S \rightarrow \frac{V_G - V_t}{R_S} > I_D.$$
Substituting the expression for $I_D$ into the inequality makes it evident that the lower sign (− in the expression above) corresponds to the physically meaningful solution:

$$\frac{V_G - V_t}{R_S} > I_D \quad \rightarrow \quad \frac{V_G - V_t}{R_S} > \frac{V_G - V_t}{R_S} + \frac{1}{k_n R_S^2} \pm \frac{1}{k_n R_S^2} \sqrt{1 + 2k_n R_S (V_G - V_t)}$$

$$\rightarrow \quad 0 > \frac{1}{k_n R_S^2} \pm \frac{1}{k_n R_S^2} \sqrt{1 + 2k_n R_S (V_G - V_t)}$$

$$\rightarrow \quad \frac{1}{k_n R_S^2} < \pm \frac{1}{k_n R_S^2} \sqrt{1 + 2k_n R_S (V_G - V_t)}$$

The lower sign is correct; it is “+” here but “−” in the original formula. Thus,

$$I_D = \frac{V_G - V_t}{R_S} + \frac{1}{k_n R_S^2} - \frac{1}{k_n R_S^2} \sqrt{1 + 2k_n R_S (V_G - V_t)}.$$

A plot of this expression for $I_D$ versus $k_n$ shows that the drain current is relatively insensitive to this parameter. Changes in the threshold voltage $V_t$ cause larger corresponding changes in $I_D$. However, the changes are much less severe than if the source resistor $R_S$ were not present.

The complicated expression for $I_D$ derived above does not suggest a straightforward approach for selecting values of $V_G$ and $R_S$ to achieve a target bias level. Furthermore, the voltage transfer characteristic for this circuit, even with a source degeneration resistor, is nonlinear. It is therefore difficult to determine an optimum value to which the quiescent drain voltage $V_D$ and/or the quiescent drain current $I_D$ should be set. Because of the square-law nature of the relationship between $I_D$ and $V_{GS}$, the output voltage swing is not symmetrical. In practice, many designers turn to a common rule of thumb in which the voltage across $R_D$, the drain-source voltage $V_{DS}$, and the voltage across $R_S$ are each set equal to one-third of $V_{DD}$. That is,

$$I_D R_D = V_{DS} = I_D R_S = \frac{1}{3} V_{DD}.$$

Values for $R_D$ and $R_S$ can be found directly from this if a target value of $I_D$ is specified. The appropriate value of the quiescent gate voltage $V_G$ can then be found by once again combining the relationships

$$I_D = \frac{1}{2} k_n (V_{GS} - V_t)^2 \quad \text{and} \quad V_{GS} = V_G - I_D R_S,$$

but this time solving for $V_G$, which leads to

$$I_D = \frac{1}{2} k_n (V_G - I_D R_S - V_t)^2$$

$$V_G - I_D R_S - V_t = \sqrt{\frac{2I_D}{k_n}}$$

$$V_G = I_D R_S + V_t + \sqrt{\frac{2I_D}{k_n}}.$$
The positive value of the square root is used because it corresponds to the requirement that $V_{GS} > V_t \rightarrow V_G - I_D R_S > V_t$. Of course, this method for selecting the value of $V_G$ depends on knowing the values of $k_n$ and $V_t$, which vary considerably because of manufacturing tolerances and temperature effects. (The parameters $\mu_n$ and $V_t$ are especially sensitive to temperature.) It is therefore difficult, if not impossible, to set a quiescent drain current value that is repeatable from circuit to circuit. Bear in mind, however, that the presence of the source degeneration resistor $R_S$ will force the drain current to remain close to whatever value it happens to have. Thus, even though we cannot set $I_D$ to a specific value with much precision, we can make sure that it has negligible drift. In practice the nominal values of $k_n$ and $V_t$, obtained either from a data sheet or via measurements, are used to set $V_G$. Since the value of $V_{GS}$ must be greater than $V_t$ in order to avoid the cut-off region, it is often advisable to set $V_G$ slightly higher than the value suggested by the formula above. The voltage divider network formed by $R_A$ and $R_B$ establishes the value of $V_G$ in the circuit. Since zero current flows into the gate, $V_G$ is related to $V_{DD}$ by

$$V_G = V_{DD} \frac{R_B}{R_A + R_B} \Rightarrow \frac{R_B}{R_A} = \frac{V_G}{V_{DD} - V_G}.$$ 

The parallel combination of the gate biasing resistors (i.e., $R_A || R_B$) is typically set to a large value (1 MΩ or more) in order to maintain a high input impedance for the amplifier.

In many design situations the actual value of $I_D$ is less important than ensuring that the MOSFET operates in the saturation region. Circuits like the one shown in Figure 1 are usually used to amplify only very small input signals (i.e., having peak-to-peak amplitudes of a few mV or less) represented by the voltage source $v_g$. In those cases the output voltage swing, and therefore the drain current swing, will be tiny compared to the corresponding quiescent values (a few millivolts vs. a few volts). Although the voltage transfer characteristic of a MOSFET amplifier is nonlinear, it is approximately linear over small portions of the saturation region. The small-signal voltage gain is equal to the slope of the transfer characteristic at the Q-point. If the actual quiescent output voltage differs from its intended value, the small-signal voltage gain will differ from the target value as well, but usually the difference is not too great and can be tolerated in a practical circuit. If many copies of a circuit are needed with predictable bias levels, then it might be necessary to screen the stock of MOSFETs that will be used in the production of the circuit to eliminate those devices that have parameters outside the acceptable limits. If very precise bias control is required, however, then other types of biasing circuits should be used, such as those based on constant-current sources (e.g., current mirrors).

**Experimental Procedure**

- Devise a way to determine the parameters $V_t$ and $k_n$ for the 2N7000 n-channel enhancement mode MOSFET from the data sheet available on the Laboratory page of the course web site. There are many ways to do this, and if you try more than one you will probably find that they lead to different values for $k_n$. However, all of them should lead to values that are within 20-50% or so of each other. This wide variation is not a major concern because the bias circuit you will be designing compensates for variations in parameter values. (It is especially effective at addressing variations in the value of $k_n$.) Furthermore, the resistors have 5% tolerances, so some variation in bias levels is to be expected anyway.

- Verify with the instructor that your calculated parameter values are within reason.
• Design a four-resistor bias circuit like the one shown in Figure 1 (i.e., find values for $R_D$, $R_S$, $R_A$, and $R_B$) for a 2N7000 MOSFET. Assume that the design specification calls for a power supply voltage $V_{DD}$ of 12 V, a quiescent drain current of $I_D = 10$ mA, and a quiescent drain voltage of $V_D = 8$ V (measured with respect to ground). Use a reasonable rule of thumb for the quiescent voltage across $R_S$. Base your design on the values for $V_t$ and $k_n$ you deduced from the data sheet. Each resistor should be a single unit with the standard value closest to the calculated value. For the gate biasing resistors, use values in the high hundreds of kΩ or MΩ range. Verify that the power dissipation limits for the MOSFET and for the resistors will not be exceeded. If any of the resistors’ ratings would be exceed, you may use multiple resistors to distribute the dissipation load. Record your bias design process for inclusion in your report.

• Insert three different 2N7000 MOSFET from the available stock into the four-resistor bias circuit, and measure the quiescent drain voltage $V_D$ for each one. In each case, calculate the percentage error by which the measured value of $V_D$ differs from the target value. Warm each MOSFET either by holding it between your fingers or by using a hair dryer until the value of $V_D$ stabilizes. Record the new $V_D$ value at the higher temperature, and calculate the percentage departure from the target value. You should finish with six measured $V_D$ values, two for each MOSFET. Comment on the stability of the bias circuit relative to device variation and temperature change.

• Demonstrate your properly operating bias circuit for one of the MOSFETs to the instructor.

• Build the circuit shown in Figure 2 using the same value for $R_D$ as you used in your four-resistor bias circuit. Insert one of the MOSFETs into the circuit, and adjust the value of $V_{GS}$ (you may use the 6-V supply) until $V_D = 8$ V. Note that the quiescent values of $V_D$ and $I_D$ are approximately the same in this circuit as in the four-resistor circuit. Warm the MOSFET until the value of $V_D$ stabilizes, and then measure the new value of $V_D$. Compare the temperature stability of this circuit to that of the four-resistor bias circuit.

![Figure 2. MOSFET bias circuit without source degeneration.](image)

• Demonstrate the behavior of the simple circuit shown in Figure 2 to the instructor.
Grading

The lab group member(s) identified for writing assessment must submit a brief but well written report that describes in detail all circuit design choices, assembly steps, test configurations, and the results of measurements. The report should include (but not necessarily be limited to) all of the details requested in the “Experimental Procedure” section.

The report is due at the beginning of next week’s lab session. The group member(s) who writes the report will receive a grade with a starting value of 50% with the following maximum possible percentages added:

30% Report – Completeness and technical accuracy
10% Report – Organization, neatness, and style (professionalism)
10% Report – Spelling, grammar, and punctuation

The group member(s) who will not be writing a report must submit a short explanation of how the values of $V_t$ and $k_n$ were determined. This/these group member(s) will receive a grade with a starting value of 50% with the following maximum possible percentages added:

10% Determination of reasonable values for $k_n$ and $V_t$
30% Demonstration of a properly operating four-resistor bias network
10% Demonstration of a simple bias network

Of course, any group member who misses the lab session and is not excused will receive a grade of zero.