Introduction

The design of most MOSFET amplifiers is divided into the separate tasks of biasing and small-signal modeling. Biasing is the adjustment of the quiescent DC voltages and currents in the circuit so that the positive and negative excursions of the applied input signal do not cause the transistor to enter the triode or cutoff regions. In a linear amplifier, in which the output signal is intended to be a magnified replica of the input signal, it is necessary to keep the transistor operating in the saturation (constant-current) region at all times. The biasing of an amplifier amounts to solving a DC problem, whereas small-signal modeling is an AC problem. The latter task involves analyzing how a circuit responds to incremental changes in the input voltage or current and can therefore be used to determine the voltage gain or other characteristics. In this lab experiment you will investigate the small-signal modeling of a common-source MOSFET amplifier with source degeneration.

Pre-Lab Work and Quiz

There will be no quiz or pre-lab work for this lab exercise, except to read over this handout carefully before the lab session. The more familiar you are with the task ahead, the more efficiently you will be able to use your lab time.

Theoretical Background

Shown in Figure 1 is a common-source amplifier intended for use with small signals. The resistor values have been chosen to obtain the bias conditions indicated in the figure caption. (These are the same as the target bias values in the previous lab exercise.) The capacitors $C_i$ and $C_o$ isolate the amplifier at DC from the source and the load. If these capacitors were not present, then the bias voltage and current levels could be affected by the source and load. The upper capacitor labeled $C_{by}$ bypasses the power supply at signal frequencies, and the lower capacitor labeled $C_{by}$ bypasses the source degeneration resistor. All four capacitors could, of course, have an effect on the AC (small-signal) operation of the circuit, so their values are usually made large enough so that their reactances are negligible at the lowest frequency of interest (i.e., so that the signal voltage drops across them are negligible). The expression for capacitive reactance $X_C$ at frequency $f$ is given by

$$X_C = \frac{-1}{\omega C} = \frac{-1}{2\pi f C}.$$  

where $C$ is the capacitance.

To analyze the small-signal behavior of this circuit, the transistor must be replaced by its small-signal model, and all DC voltage and current sources must be set to zero. Deactivated voltage sources become shorts, and deactivated current sources become opens. The resulting small-signal model of the amplifier circuit is shown in Figure 2.
Figure 1. Common-source amplifier using an n-channel enhancement-mode MOSFET with source degeneration. The quiescent point has been set at $V_D = 8$ V and $I_D = 10$ mA for a 2N7000 type MOSFET.

The double bar (||) notation in Figure 2 indicates that a parallel combination of two resistors has been replaced in the circuit diagram by a single resistor of an equivalent value. The two circles labeled $v_{in}$ and $v_o$ represent the input and output ports of the amplifier, respectively. Devices $v_{sig}$ and $R_{sig}$ comprise the Thévenin equivalent circuit of the signal source, and $R_L$ represents the load. Resistance $R_L$ typically represents the input resistance of a following amplifying stage or a transducer such as a speaker or recording device. Note that the source and the load are not part of the amplifier circuit. The amplifier itself is comprised only of the circuitry between the input and output ports. Nevertheless, as we will see, the source and/or load circuitry can sometimes affect the voltage gain as well as the input and output resistances of the amplifier.

Figure 2. Small-signal model of the common-source amplifier. All capacitors are assumed to have negligible reactances at the operating frequency and are therefore modeled as shorts.
The quantity $g_m$ is the small-signal transconductance and is derived by considering the behavior of the MOSFET when small fluctuations are superimposed on the quiescent voltages and currents. Recall that MOSFETs used as amplifiers are almost always biased to operate in the saturation region. Thus, the drain current is related to the gate-to-source voltage via (for NMOS devices)

$$i_D = \frac{1}{2} k_n (v_{GS} - V_t)^2,$$

where $i_D$ is the total (quiescent plus signal) drain current, $v_{GS}$ is the total gate-to-source voltage, $k_n$ is the MOSFET transconductance parameter (a different transconductance from $g_m$), and $V_t$ is the threshold voltage. The drain current and gate-to-source voltage can be decomposed into their bias and signal components as

$$i_D = I_D + i_d \quad \text{and} \quad v_{GS} = V_{GS} + v_{gs},$$

where a lower-case variable/upper-case subscript indicates a total quantity; upper-case/upper-case indicates a bias quantity; and lower-case/lower-case indicates a small-signal quantity. Substituting these relations into the $i$-$v$ characteristic yields

$$I_D + i_d = \frac{1}{2} k_n (v_{GS} + v_{gs} - V_t)^2.$$

This expression can be manipulated to separate the bias effects from the small-signal effects:

$$I_D + i_d = \frac{1}{2} k_n \left[(v_{GS} - V_t) + v_{gs}\right]^2$$

$$= \frac{1}{2} k_n \left[(v_{GS} - V_t)^2 + 2(v_{GS} - V_t)v_{gs} + v_{gs}^2\right].$$

Making the assumption that $v_{gs}^2 \ll 2(v_{GS} - V_t)$, which is the criterion that establishes the meaning of “small signal,” then the $v_{gs}$ term in the brackets can be ignored. The expression then becomes

$$I_D + i_d \approx \frac{1}{2} k_n \left[(v_{GS} - V_t)^2 + 2(v_{GS} - V_t)v_{gs}\right]$$

$$= \frac{1}{2} k_n (v_{GS} - V_t)^2 + k_n (v_{GS} - V_t)v_{gs}.$$

The first term on the right has no signal quantities, whereas the second term on the right has the signal quantity $v_{gs}$. The right-hand side is thus clearly decomposed into quiescent and small-signal parts, so

$$I_D = \frac{1}{2} k_n (v_{GS} - V_t)^2 \quad \text{and} \quad i_d = k_n (v_{GS} - V_t)v_{gs}.$$

The first expression is the familiar relationship between the quiescent drain current and the quiescent gate-to-source voltage for operation in the saturation region. The second expression
provides a very accurate relationship between the small-signal drain current and the small-signal gate-to-source voltage. It implies that if \( V_{GS} \) is constant (as it should be if the bias design is done properly!), then \( i_d \) is linearly related to \( v_{gs} \). The proportionality constant is represented by the quantity \( g_m \). That is,

\[
i_d = g_m v_{gs}, \quad \text{where} \quad g_m = k_n (V_{GS} - V_t).
\]

This suggests that the small-signal drain current can be modeled as a voltage-controlled current source with a “gain” factor \( g_m \). That is indeed how \( i_d \) is modeled in Figure 2 (and in almost all small-signal models). The expression for \( g_m \) given above implies that it is dependent on the value of the quiescent gate-to-source voltage \( V_{GS} \). However, it is often more convenient to express \( g_m \) in terms of the quiescent drain current \( I_D \) since the latter is a more natural biasing target. An alternate expression for \( g_m \) can be obtained using the relationship between \( I_D \) and \( V_{GS} \) in the saturation region:

\[
I_D = \frac{1}{2} k_n (V_{GS} - V_t)^2 \quad \Rightarrow \quad (V_{GS} - V_t) = \sqrt{\frac{2I_D}{k_n}}.
\]

Substituting this into the original expression for \( g_m \) yields

\[
g_m = k_n (V_{GS} - V_t) = k_n \sqrt{\frac{2I_D}{k_n}} \quad \Rightarrow \quad g_m = \sqrt{2k_n I_D}.
\]

A typical goal in amplifier analysis is to derive the voltage gain \( v_o/v_{in} \). This task is easily accomplished using the small-signal model. (We will soon see why we are not deriving \( v_o/v_{sig} \) here.) First, referring to Figure 2, note that the dependent current source draws current from the ground through the parallel combination of resistors \( R_D \) and \( R_L \). The output voltage is therefore given by

\[
v_o = -(g_m v_{gs}) (R_D || R_L).
\]

In any expression involving a parallel combination of resistances (or impedances), the parallel operation takes precedence over multiplication. Thus, the expression for \( v_o \) can be clarified without changing its meaning by rewriting it without parentheses:

\[
v_o = -g_m v_{gs} R_D || R_L.
\]

By inspection, the input voltage \( v_{in} \) is equal to the small-signal gate-to-source voltage \( v_{gs} \). That is, \( v_{in} = v_{gs} \). The expression for the small-signal voltage gain \( A_v \) of the amplifier is therefore

\[
A_v \equiv \frac{v_o}{v_{in}} = -\frac{g_m v_{gs} R_D || R_L}{v_{gs}} \quad \Rightarrow \quad A_v = -g_m R_D || R_L.
\]

One of the implications of this result is that the voltage gain of the amplifier is a function of the load resistance \( R_L \). The reason for this is obvious if the amplifier and its source and load are modeled using Thévenin equivalent circuits as shown in Figure 3. The parameter \( A_{vo} \) in the voltage-dependent voltage source in Figure 3 is the “open-circuit” gain of the amplifier; that is, it
represents the gain obtained when the output of the amplifier is connected to an open circuit (an infinite load resistance). In the case of the common-source amplifier we are considering here,

\[ A_{vo} \equiv \left. \frac{v_o}{v_{in}} \right|_{R_L \to \infty} = -g_m R_D. \]

\[ R_{in} \]

\[ v_{in} \]

\[ i_{in} \]

\[ R_{sig} \]

\[ v_{sig} \]

\[ R_{in} \]

\[ A_{vo} v_{in} \]

\[ R_{o} \]

\[ v_{o} \]

\[ R_{L} \]

Figure 3. Model of amplifier using four Thévenin equivalent circuits to represent the source, the input of the amplifier, the output of the amplifier, and the load.

The amplifier has an output resistance \( R_o \), which is the Thévenin equivalent resistance of the amplifier’s output port. If \( R_L \) is finite, then the Thévenin equivalent voltage \( A_{vo} v_{in} \) is divided between \( R_o \) and \( R_L \). A similar situation occurs at the input of the amplifier. The source (signal) voltage \( v_{sig} \) is divided between the source resistance \( R_{sig} \) and the input resistance of the amplifier \( R_{in} \). However, if \( R_{sig} \ll R_{in} \), then \( v_{in} \approx v_g \). That is why voltage amplifiers are often designed with as large an input resistance (or impedance) as possible; if \( R_{in} \) is large enough, then only a negligible portion of \( v_{sig} \) is “lost” due to voltage division.

This brief discussion of input and output resistances is for illustrative purposes only. You will not have to attempt to analyze or measure either quantity in this lab exercise. However, both concepts will be examined in great detail in ELEC 351.

**Experimental Procedure**

- Assemble a common-source amplifier circuit with a 2N7000 n-channel MOSFET and the resistor and power supply values shown in Figure 1. Note that \( R_{sig} \) is not a physical resistor; it represents the output impedance of the bench-top function generator. Use large enough values for the bypass capacitors (labeled \( C_{by} \)) so that they have reactances of a few ohms or less at 1 kHz or higher. If you use electrolytic capacitors, which are polarized, make sure they are oriented correctly in the circuit. Make the DC blocking capacitors \( C_i \) and \( C_o \) large enough so that their reactances are negligible compared to the equivalent resistances with which they are in series in the small-signal model. (“Negligible” is about 1/100 or less.) Note that \( C_i \) and \( C_o \) can be (and should be) considerably smaller than the bypass capacitors. Use of appropriately sized capacitors for \( C_i \) and \( C_o \) will be viewed positively.
• Verify by measurement that the quiescent voltages and currents listed in the caption of Figure 1 are close to their design values in your circuit. These measurements must be taken with no source voltage $v_{\text{sig}}$ applied to the amplifier. If the bias levels are way off, make reasonable adjustments to the resistor values. Note that changing one of the resistor values will affect the gain; avoid making changes to that value.

• Estimate by analysis the voltage gain ($v_o/v_{\text{in}}$) of the amplifier. Obtain a rough estimate of the parameter $k_n$ (which you will need) by making use of information given in the 2N7000 data sheet or by using your notes from the previous lab exercise. If you need the threshold voltage $V_t$, estimate it as well using information from the data sheet. Be sure to explain where and/or how you obtained the data you used.

• Use the function generator to apply a 1-kHz sine wave to the input of the amplifier, and use the oscilloscope to monitor the voltages $v_{\text{in}}$ and $v_o$ simultaneously. Adjust the generator so that the output voltage is an undistorted sine wave with a peak magnitude of 100 mV or so.

• Demonstrate your operating amplifier to the instructor or TA.

• Capture a screen image of the input and output voltage waveforms, and determine the voltage gain from your measurements. Use the “BW Lim” feature to minimize noise on the waveforms. Remember, if the amplifier inverts the input signal, then the gain is negative. Compare the measured gain to the estimated gain determined earlier by analysis, and comment on the results.

• Increase the signal level until either the top or the bottom of the output sine wave begins to distort, and note the peak signal ($v_{\text{sig}}$) and output ($v_o$) voltage levels at which this occurs. Capture a screen image of the output waveform experiencing distortion at this extreme. Now continue to increase the signal level until the other extreme of the output waveform begins to distort, and note those peak signal and output voltage levels as well. Capture a screen image of the output waveform experiencing distortion at both extremes. Based on your observations, do you think the quiescent bias point was set closer to the edge of cutoff or the edge of the triode region? Explain your answer.

Grading

The lab group member(s) identified for writing assessment must submit a brief but well written report that describes in detail all circuit design choices, assembly steps, test configurations, and the results of measurements. The report should include (but not necessarily be limited to) all of the details requested in the “Experimental Procedure” section.

The report is due in Dana 301 at 6:00 pm (hard copy) or via e-mail at 11:59 pm (PDF copy) on December 3, 2012. The group member(s) who writes the report will receive a grade with a starting value of 50% with the following maximum possible percentages added:

30% Report – Completeness and technical accuracy
10% Report – Organization, neatness, and style (professionalism)
10% Report – Spelling, grammar, and punctuation

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The group member(s) who will not be writing a report must submit 1) a short outline of how the voltage gain of the amplifier was calculated using circuit analysis, and 2) a copy of the screen capture of the output waveform showing distortion at its positive and negative extremes with the intervals of operation in the cutoff and triode regions clearly indicated. The summary is due in Dana 301 at 6:00 pm (hard copy) or via e-mail at 11:59 pm (PDF copy) on December 3, 2012. This/these group member(s) will receive a grade with a starting value of 50% with the following maximum possible percentages added:

10% Proper voltage gain calculations
10% Properly labeled screen capture of distorted output waveform
30% Demonstration of a properly operating amplifier circuit

Any group member who misses the lab session and is not excused will receive a grade of zero.

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