Introduction

The piecewise linear model of the pn-junction diode under forward bias conditions consists of a resistor in series with an independent voltage source. The value of the series resistance depends on the diode current, a property that can be exploited to design a remotely controlled attenuator circuit. Attenuation is a reduction in signal strength. Attenuation can be undesirable, as in the case of long distance data communication, or it can be introduced on purpose, for example, to protect sensitive equipment from strong signals or to implement a volume control.

In this two-part lab exercise you will design and test a simple attenuator circuit and use it to control the amplitude of a sinusoidal signal. The first step, which will be completed this week, is to design a circuit to supply a voltage that varies from roughly 0.5 V to roughly 12 V. While this could be accomplished using a potentiometer and a handful of other components, a more modern approach is to use up/down pushbutton controls. Therefore, in the first part of the lab exercise, you will implement a variable voltage circuit using a binary up/down counter and a multi-input scaling and level-shifting circuit based on an op-amp.

Theoretical Background

The control circuitry that will supply the variable voltage has two main sections. The first is a pre-assembled binary up/down counter that creates a 4-bit digital signal with 16 possible values. The heart of the circuit is a 74HC193 4-bit up/down counter IC. The second section, which you will have to design and assemble, is a digital-to-analog (D/A) converter that produces an output voltage specified by the 4-bit input. Most D/A converters produce voltages that range from zero to some maximum value. However, this application requires that the minimum voltage be about 0.5 V instead of zero. Thus, you will make use of a summing amplifier to produce the desired range of voltages while also introducing an appropriate amount of level-shifting. The range of voltages you will need to generate is listed in Table 1 on the next page.

Binary Counter Circuit

Shown in Figure 1 on Page 3 is the schematic diagram of the counter circuit. The 78LS05 is a voltage regulator that produces a steady DC output of +5 V relative to ground. The 5-V source is distributed to the other integrated circuits, which are CMOS (complementary metal-oxide semiconductor) devices. The 74HC193 produces a 4-bit digital output signal (present at pins 2, 3, 6, and 7 and labeled $Q_A$ through $Q_D$ in the diagram) that represents a logical 0 using 0 V and a logical 1 using 5 V. Output $Q_A$ is the least significant bit, and $Q_D$ is the most significant bit. The 4-bit output varies from 0000 to 1111 under control of the “down” and “up” signals applied to pins 4 and 5, respectively. Pins 4 and 5 are normally resting high (i.e., logical 1 or 5 V). An increment or decrement in the 4-bit binary output occurs when the “up” or “down” pin goes low (0 V) and then goes high (5 V) again.
Table 1. Output voltages of scaling and level-shifting circuit for all possible binary inputs.

<table>
<thead>
<tr>
<th>Binary Number</th>
<th>Decimal Equivalent</th>
<th>Output Voltage (V)</th>
</tr>
</thead>
<tbody>
<tr>
<td>0000</td>
<td>0</td>
<td>0.50</td>
</tr>
<tr>
<td>0001</td>
<td>1</td>
<td>1.25</td>
</tr>
<tr>
<td>0010</td>
<td>2</td>
<td>2.00</td>
</tr>
<tr>
<td>0011</td>
<td>3</td>
<td>2.75</td>
</tr>
<tr>
<td>0100</td>
<td>4</td>
<td>3.50</td>
</tr>
<tr>
<td>0101</td>
<td>5</td>
<td>4.25</td>
</tr>
<tr>
<td>0110</td>
<td>6</td>
<td>5.00</td>
</tr>
<tr>
<td>0111</td>
<td>7</td>
<td>5.75</td>
</tr>
<tr>
<td>1000</td>
<td>8</td>
<td>6.50</td>
</tr>
<tr>
<td>1001</td>
<td>9</td>
<td>7.25</td>
</tr>
<tr>
<td>1010</td>
<td>10</td>
<td>8.00</td>
</tr>
<tr>
<td>1011</td>
<td>11</td>
<td>8.75</td>
</tr>
<tr>
<td>1100</td>
<td>12</td>
<td>9.50</td>
</tr>
<tr>
<td>1101</td>
<td>13</td>
<td>10.25</td>
</tr>
<tr>
<td>1110</td>
<td>14</td>
<td>11.00</td>
</tr>
<tr>
<td>1111</td>
<td>15</td>
<td>11.75</td>
</tr>
</tbody>
</table>

The “up” and “down” signals are generated by the corresponding pushbuttons shown near the top of the diagram. Momentary contact pushbuttons like these typically suffer from a phenomenon known as “bounce,” which means that when pushed and released they do not simply close and then open again but instead open and close several times over the course of a few tens of milliseconds. The circuit therefore reacts as if the button had been pushed several times in rapid succession. This makes it almost impossible to obtain one count for one pushbutton press. To solve the problem, a Schmitt trigger (the NOT gate symbol with what looks like a double integral sign but actually is a representation of a property called hysteresis) is added to each pushbutton. The output of the Schmitt trigger remains low (logical 0) until the button is pressed. That action discharges the 1-μF capacitor to ground through the 18-kΩ resistor, which applies a low signal to the trigger’s input and causes the trigger’s output to go high (logical 1) very quickly (with a time constant of 18 ms). When the switch bounces and opens again, the capacitor does not charge up to 5 V immediately. Instead, its charge rate is governed by the time constant set by the 82-kΩ and 18-kΩ resistors and 1-μF capacitor (100 ms). The time constant is much longer than the time between bounces, so the input to the trigger remains low (does not make a transition to high) as long as the button is pressed. When the button is released, the trigger’s output goes low only after the capacitor’s voltage almost reaches 5 V.

The 74HC154 4-to-16 line decoder/demultiplexer chip indicates the value represented by the 4-bit output of the 74HC193 by lighting the correct corresponding LED. The outputs of the 74HC154 are active-low, meaning that they are normally high. An individual output goes low only if its associated value is applied to the 4-bit input on pins 20-23. For example, if the binary input is 1001, then the output associated with the value 9 (pin 10) goes low. An LED can light only if the voltage across it and the 1-kΩ current limiting resistor is greater than roughly 2 V, so if the pin an LED is connected to is high, that LED will remain off.
Figure 1. Binary counter circuit that generates a 4-bit incrementing or decrementing digital signal under manual control and displays the current binary value by lighting one of 16 LEDs (adapted from [1]). LSB = least significant bit; MSB = most significant bit. The small triangles represent ground connections.

Another feature of the circuit is that it prevents the “wrap-around” effect in which the counter cycles from 1111 back to 0000 if the “up” button is pressed repeatedly or from 0000 to 1111 if the “down” button is pressed repeatedly. That is, the counter will not decrement or increment...
beyond the 0000 or 1111 limit, respectively. For example, if the “up” button is pressed when the
counter is at 1111, the logical 0 at pin 17 of the 74HC154 will cause one of the input pins of the
74HC00 NAND gate connected to pin 5 (“up”) of the 74HC193 to be low. This prevents the
output of the 74HC00 from going low regardless of the state of the pushbutton; therefore, the
“up” pin cannot be clocked. (The output of a NAND gate is 0 only if both inputs are 1.)

**D/A Converter with Offset**

The output voltages at pins 2, 3, 6, and 7 (labeled $Q_A$ through $Q_D$) of the 74HC193 are very close
to zero when in the low state and very close to 5 V when in the high state. This predictability
allow us to use the circuit shown in Figure 2 to convert the 4-bit digital signal into an attenuator
control voltage that varies over a wide range in equal increments. You should recognize the left
side of the circuit as being similar to a summing amplifier. The only difference is the presence of
an offset voltage $V_{\text{off}}$ in the noninverting input lead, which introduces a “floor” (a constant
minimum) for the output voltage. Note that $V_{\text{off}}$ is an externally applied voltage; it does not
represent the input offset voltage. Without that voltage source, the output of the summing
amplifier would be 0 V for a digital input of binary 0000. The right side of the circuit is a
standard inverter. It is necessary because the summing amplifier produces a negative output
voltage if the four inputs are positive. The choice of power supply voltages (±15 V in this case)
is somewhat arbitrary; however, the desired output voltage range of each op-amp must lie
between the two supply voltages with approximately 2 V to spare at each limit.

\[
\begin{align*}
V_{\text{BIAS}} &= \frac{R_2}{R_1} \left[ \frac{R_f}{R_D} v_D + \frac{R_f}{R_C} v_C + \frac{R_f}{R_B} v_B + \frac{R_f}{R_A} v_A \right. \\
&\quad \left. - \left( 1 + \frac{R_f}{R_B} \frac{R_f}{R_C} \frac{R_f}{R_D} \right) V_{\text{off}} \right].
\end{align*}
\]

**Figure 2.** Multi-input scaling and level-shifting circuit designed to convert a 4-bit
digital signal into a variable voltage at node $V_{\text{BIAS}}$. LSB = least significant bit;
MSB = most significant bit. The small triangles represent ground connections.

It is relatively easy to show that the output voltage of the complete circuit in Figure 2 is given by
(you should verify this; the easiest way is via superposition)
The input voltages $v_A$ through $v_D$ correspond to the four bits of the binary signal produced by the 74HC193 labeled $Q_A$ through $Q_D$. A logical 0 is represented by 0 V, and a logical 1 is represented by the positive power supply voltage of +5 V (which differs from the voltages driving the op-amps). Input voltage $v_A$ represents the least significant bit (LSB) and $v_D$ the most significant bit (MSB). Input resistors $R_A$ through $R_D$ must be chosen so that a change in state in the bit applied to the corresponding input causes an appropriate change in the output voltage. For example, for a circuit designed to produce the outputs given in Table 1, if $v_A$ changes from logical 0 to logical 1, the output voltage must rise by 0.75 V. Likewise, if $v_D$ changes from 0 to 1, the output voltage must rise by 6 V. Note that the voltage increments corresponding to the various inputs are related to each other by powers of two. The value of $R_f$ along with those of $R_1$ and $R_2$, set the extent of the output voltage range (0.5-11.75 V in this case) obtained for the full range of input binary numbers between 0000 and 1111.

**Experimental Procedure**

- You will be given a pre-assembled 4-bit up/down binary counter circuit based on the 74HC193 like the one shown in Figure 1. Test the circuit and make sure you understand how it interfaces to the D/A converter circuit and how power will be supplied to it (including the reference node connection). Check for proper operation of the counter circuit before proceeding to the next step.

- Determine appropriate resistor values and the value of $V_{off}$ for the 4-bit D/A converter (DAC) and level shifter shown in Figure 2 so that it produces the output voltages given in Table 1 for the 16 possible digital inputs. Assume that a logical 0 bit is represented by 0 V and a logical 1 bit is represented by +5 V. The power supply voltages for the op-amps should be ±15 V. For the input resistors $R_A$ through $R_D$, use standard values that are large enough to avoid sourcing or sinking excessive output current from the op-amps but that are small enough to minimize errors due to input bias currents. Do not use multiple resistors in series or parallel to create nonstandard values; each resistor in Figure 2 should be implemented using one physical component to achieve a clean and compact design. A wide range of valid choices can be made for the values of resistors $R_f$, $R_1$, and $R_2$. Your choices should be guided by scaling the output properly, avoiding clipping, and minimizing the effects of input bias currents and input offset voltages. Voltage source $V_{off}$ may be implemented in any way that works. However, you should try to devise a more creative solution than simply using the 6-V power supply (5 points of extra credit if you do!).

Because you must use standard values for all of the resistors in your circuit, you might not be able to create the exact resistor ratios that you need. Try to get as close as possible to your design values, but do not spend too much time working out a solution. After all, the resistors available in the lab do not have very tight tolerances (5% in most cases). Also, the attenuation accuracy you will have to achieve next week will not be very stringent.

- Assemble the D/A converter and level shifter according to your design, and connect it to the 4-bit binary counter. Be sure that all circuits and power supplies have a common reference node (ground).

- Validate the proper operation of the circuit by measuring the output voltages obtained for the various binary input combinations and ensuring that they are close to the values given in
Table 1. A match that is within 10% or so of the target value is acceptable. Check whether the four input voltages are either 0 V or 5 V as originally assumed. Record the actual voltages, and note if they differ significantly from the assumed values. You should also note any unusual or unexpected circuit behaviors that you observe.

- Demonstrate your properly operating circuit to the instructor or TA.

- Record the actual output voltages measured for each of the 16 input states, and calculate the percentage errors between the desired and measured output voltages for each state. This data should be included in your lab summary in the form of a well constructed table.

Reference


Lab Summary

After your group has completed the assigned tasks and demonstrated a working circuit, prepare a written summary (one per group) no more than two pages long that includes but is not necessarily limited to the following elements:

a. Schematic diagram of the D/A converter and level shifter with all components labeled.
b. Brief description of the measurement procedure, including equipment used.
c. A comparison in tabular form of the measured and target output voltages for each of the 16 input states, along with the percentage error for each voltage. The table should have a caption and should be clear enough to allow the reader to understand the results without consulting the text (but the text should be there nevertheless).
d. Interpretation of results and observations, including any discrepancies or close agreements noted and any important circuit behavior quirks, and discussion of implications. Your ideas should be original and focus on outcomes that are new to you, not quite what was expected, or at least not obvious.

The summary should be thorough, clear, concise, and professional in tone and style. It does not have to be word-processed, but it should be easy to follow and as neat and well organized as possible. If it is word-processed, the font should be 11 points or larger, and the margins should be at least one inch wide. Single line spacing is acceptable. Equations, diagrams, and tables may be generated by hand, or you may use software. Pay especially close attention to the issues addressed in the “Lab Summary Guidelines” available at the lab web site.

You may use memo format for your summary if you wish, but you do not have to. A cover sheet is not necessary. The identifying information on the first page should include the group members’ names, the course number (ELEC 350), the lab section (Monday or Wednesday), the lab number, and the lab date (not the summary due date).
Grading

Each group member will receive the same grade based on the following criteria. Scores will be quantized at the indicated percentage levels.

0, 10, 20, 30% Properly assembled D/A and level-shifting circuit
0, 10, 20, 30, 40% Demonstration of fully operational circuit that meets specifications
0, 5, 10, 15, 20% Summary – Completeness and technical accuracy
0, 3, 5% Summary – Organization, neatness, and style (professionalism)
0, 3, 5% Summary – Spelling, grammar, and punctuation

As outlined in the lab policies and guidelines, any group member who misses any portion of the lab session and is not excused will receive a grade penalty proportional to the time absent.

If the demonstration is not completed by the end of the lab session, full demonstration credit can be obtained if the circuit is made to operate and a detailed one-page explanation of the problem and its solution is provided within 24 hours. The explanation is separate from the lab summary.

The lab summary is due at the beginning of next week’s lab session. Summaries submitted after the deadline but before 6 pm on the following day will result in a 20% grade deduction applied to the lab grade. No credit will be given for a summary submitted later, although credit for successful assembly and demonstration of the assigned circuit will still be given.

Group Assignments

The randomly generated groups for this lab exercise are listed below. They will remain the same for Lab #5:

Monday section
DAbbraccio-Kaspar
Hontz-Hough
Goesseringer-Ludwig
MacGibbon-Gegg
Brown-Rocci-Daughan

Wednesday section
Ononuju-Bekampis
Sommers-Moore
Bennett-Carno
Mylet-Breen
Kwiatkowski-Clark
Bacon-Opalinski

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