Lab #7: Voltage Regulation Using a Zener Diode

Introduction

Simple DC power supplies that consist only of a transformer, full-wave rectifier, and filter capacitor are adequate for many practical applications. However, this basic circuit has several important disadvantages: 1) the capacitors required to reduce the ripple voltage to a small magnitude are physically large and expensive; 2) even with minimal ripple, the output voltage can vary considerably due to AC line voltage fluctuations; 3) the secondary winding of the transformer must be selected or designed to provide the desired output voltage; and 4) changes in load current can lead to changes in output voltage due to the voltage drops across the internal resistances of the rectifier diodes and transformer windings. These deficiencies can be addressed through the use of a voltage regulator circuit, which maintains the output voltage of the power supply close to a predetermined level regardless of component and load variations. Zener diodes, which exhibit very stable voltages across themselves when operated in the reverse breakdown region, can serve as simple yet effective voltage regulators in a wide range of applications. In this lab exercise you will design one such circuit.

Theoretical Background

All diodes exhibit reverse breakdown behavior when subjected to a reverse-bias voltage of sufficiently high magnitude. Reverse breakdown is not necessarily destructive. While it is normally associated with ratings being exceeded in standard pn-junction diodes, zener diodes, by contrast, are designed to operate in this mode safely. As shown in the $i$-$v$ characteristic in Figure 1, the reverse breakdown region is marked by the zener voltage, $V_Z$.

![Zener diode $i$-$v$ characteristic](image)

Figure 1. Zener diode $i$-$v$ characteristic.
A zener diode behaves like a standard pn-junction diode in the reverse-bias and forward-bias regions because the \(i-v\) characteristic obeys the familiar diode equation for \(v_D > -V_Z\). However, for \(v_D < -V_Z\), where the diode operates in the reverse breakdown region, the slope of the \(i-v\) curve is much steeper than it is in the forward-bias region. This implies that the voltage across the diode remains very close to \(-V_Z\) in reverse-breakdown mode, regardless of the level of diode current. This characteristic makes the zener diode useful as a voltage regulator. If a load is connected in parallel with a diode operating in reverse breakdown mode, then the voltage across the diode, and therefore the voltage across the load, will remain very close to \(V_Z\).

A typical power supply circuit that employs a zener diode as a voltage regulator is shown in Figure 2. The circuit has a filter capacitor, but its value does not have to be as large as the one in an unregulated supply because the zener diode effectively smoothes out most of the ripple.

![Figure 2. Full-wave bridge rectifier circuit with filter capacitor and zener diode voltage regulator. Resistor \(R_b\) is a “bleeder” resistor that ensures capacitor \(C\) quickly discharges when the power is shut off, even if the load is an open circuit.](image)

The design procedure for this type of circuit differs from that used for the basic full-wave circuit. Most regulated power supplies are designed to provide a constant output voltage for a wide range of load currents up to some maximum value. The output voltage is equal to the zener voltage, so the output voltage specification dictates the value of \(V_Z\). The next component value to be set is usually the peak voltage of the secondary winding of the transformer. One commonly used rule-of-thumb is to set it to a value approximately 30-50% (or more) higher than the desired output voltage. Recall that the voltage across the filter capacitor approximately equals the peak voltage of the secondary minus two diode voltage drops. The 30-50% rule-of-thumb helps to ensure that there is enough voltage “headroom” between the output voltage of the rectifier/filter capacitor circuit (labeled \(v_C\) in Figure 2) and the zener voltage. This buffer is necessary to ensure that sufficient current flows through the zener diode to keep it in the reverse-breakdown region even at maximum load current in spite of component variations and possible fluctuations in the AC line voltage. [Note: In this lab exercise, the secondary voltage is dictated by the lone transformer type that is available.]

Recall that during most of the AC cycle the four rectifier diodes are off. Thus, most of the time the capacitor is supplying the current \(i_S\) that is shared between the zener diode and the load (plus an insignificantly small amount that flows through \(R_b\)). By KCL,

\[
i_S = i_Z + i_L.
\]
We also note that

\[ i_s = \frac{v_C - V_Z}{R_S}, \]

where \( v_C \) is the voltage across the capacitor, and \( V_Z \) (which equals \( v_o \)) is the zener voltage. The capacitor voltage must be maintained above \( V_Z \) to ensure that the load receives sufficient current for its needs and that the zener diode conducts enough current to remain in the reverse breakdown region. As shown in Figure 3 below, the capacitor voltage \( v_C \) has some ripple, which means that \( i_s \) varies as well. If \( v_C \) is allowed to drop to a value close to \( V_Z \) (i.e., if the ripple is very large), then \( R_S \) will have to be very small to allow sufficient current \( i_s \) to flow into the zener diode and the load at those instances. However, if \( R_S \) is too small, then at the peaks of \( v_C \) (at \( V_{\text{max}} \)) an excessive amount of current would flow through the zener diode. This is because the load draws a relatively constant current \( i_L \), at least over time scales of several periods \( T \) or more. If \( i_s \) were to increase and \( i_L \) remain constant, the zener diode would have to pass the excess current \( i_Z \). There are conflicting trade-offs here. On the one hand, a small \( C \) value (large ripple) is desirable because a small capacitor would be cheaper, smaller, and lighter than a large one. On the other hand, a large \( C \) value (small ripple) allows the value of \( R_S \) to be higher, which puts less stress on the zener diode by limiting the excess current it could potentially pass. However, a large capacitor also results in a high peak rectifier diode current.

![Figure 3. Ripple voltage across the filter capacitor in a DC power supply with a full-wave rectifier and zener diode voltage regulator. The peak voltage \( V_{\text{max}} \) is equal to the peak secondary voltage of the transformer minus two diode drops (i.e., \( v_{C,\text{pk}} \)). The period \( T \) is the reciprocal of the AC frequency \( f \). Note that \( V_Z \) is well below \( V_{\text{min}} \).](image)

A rule-of-thumb has emerged to resolve this trade-off. Designers typically select a capacitor that sets the ripple voltage to a value that is 20% of the difference between the peak capacitor voltage \( V_{\text{max}} \) and the zener voltage \( V_Z \). That is, \( V_r = 0.2(V_{\text{max}} - V_Z) \). The selection of the capacitor will be discussed in more detail later.

As mentioned earlier, the zener current \( i_Z \) has to be maintained above a certain level to ensure that the diode operates in the reverse-breakdown region. Another commonly used rule-of-thumb
is that the minimum zener current should be approximately 1/20 of the diode’s maximum safe operating current. The latter is not usually specified directly on data sheets, but it can be determined from the maximum safe power dissipation rating $P_{Z_{\text{rated}}}$, which is almost always provided. The two operating limits can therefore be determined using

$$i_{Z_{\text{max,rated}}} = \text{s.f.} \frac{P_{Z_{\text{rated}}}}{V_Z} \quad \text{and} \quad i_{Z_{\text{min,rated}}} = \frac{1}{20} \frac{P_{Z_{\text{rated}}}}{V_Z} = 0.05 \frac{P_{Z_{\text{rated}}}}{V_Z},$$

where s.f. is a safety factor that might be applied to increase the potential reliability of the circuit. Frequently, s.f. = 0.5 is used.

This leads to a guideline for determining the power rating of the zener diode for a particular application. The load current can vary from zero (if no load is connected to the power supply) up to the intended maximum $i_{L_{\text{max}}}$. If the load is drawing maximum current, then the minimum current ($i_{Z_{\text{min,actual}}}$) will flow through the zener. If the load is removed, then the maximum possible current ($i_{Z_{\text{max,actual}}}$) will flow through the zener. The difference is equal to $i_{L_{\text{max}}}$, that is,

$$i_{Z_{\text{max,actual}}} - i_{Z_{\text{min,actual}}} = i_{L_{\text{max}}}.$$

The minimum and maximum possible values of $i_Z$ must be above and below, respectively, the rated minimum and maximum values. That is, $i_{Z_{\text{min,actual}}} > i_{Z_{\text{min,rated}}}$ and $i_{Z_{\text{max,actual}}} < i_{Z_{\text{max,rated}}}$. This leads to the following constraint on the rated power dissipation:

$$i_{Z_{\text{max,rated}}} - i_{Z_{\text{min,rated}}} > i_{Z_{\text{max,actual}}} - i_{Z_{\text{min,actual}}}
\quad \rightarrow \quad i_{Z_{\text{max,rated}}} - i_{Z_{\text{min,rated}}} > i_{L_{\text{max}}}
\quad \rightarrow \quad \text{s.f.} \frac{P_{Z_{\text{rated}}}}{V_Z} - 0.05 \frac{P_{Z_{\text{rated}}}}{V_Z} = (\text{s.f.} - 0.05) \frac{P_{Z_{\text{rated}}}}{V_Z} > i_{L_{\text{max}}}
\quad \rightarrow \quad P_{Z_{\text{rated}}} > \frac{i_{L_{\text{max}}}}{\text{s.f.} - 0.05} V_Z.$$

The value of resistor $R_S$ must be chosen so that $i_S$ is high enough to supply $i_{L_{\text{max}}}$ and $i_{Z_{\text{min}}}$ at the same time, even when $v_C = V_{\text{min}}$. We therefore need to make sure that

$$i_{S_{\text{min}}} = i_{Z_{\text{min,rated}}} + i_{L_{\text{max}}}.$$

Since

$$i_S = \frac{v_C - V_Z}{R_S},$$

then the maximum value of the current-limiting resistor $R_S$ is given by

$$i_{S_{\text{min}}} = \frac{V_{\text{min}} - V_Z}{R_S_{\text{max}}} \quad \rightarrow \quad R_{S_{\text{max}}} = \frac{V_{\text{min}} - V_Z}{i_{S_{\text{min}}}} \quad \rightarrow \quad R_{S_{\text{max}}} = \frac{V_{\text{min}} - V_Z}{i_{Z_{\text{min,rated}}} + i_{L_{\text{max}}}}.$$
Using $V_{\text{min}} = V_{\text{max}} - V_r$ and the rule-of-thumb presented earlier that $V_r = 0.2(V_{\text{max}} - V_Z)$, this becomes

$$R_{S,\text{max}} = \frac{V_{\text{max}} - V_r - V_Z}{i_{Z,\text{min,rated}} + i_{L,\text{max}}} = \frac{V_{\text{max}} - 0.2(V_{\text{max}} - V_Z) - V_Z}{i_{Z,\text{min,rated}} + i_{L,\text{max}}} \rightarrow R_{S,\text{max}} = \frac{0.8(V_{\text{max}} - V_Z)}{i_{Z,\text{min,rated}} + i_{L,\text{max}}}.$$  

This sets an upper limit on the value of $R_S$, but the resistance cannot be arbitrarily small. When $i_L$ is zero, all of $i_S$ flows through the zener diode, and it reaches its peak when $v_C$ is at its peak. To ensure that the maximum safe zener current is not exceeded under no-load conditions, $R_S$ must have a minimum value given by

$$R_{S,\text{min}} = \frac{V_{\text{max}} - V_Z}{i_{Z,\text{max},\text{rated}}},$$

where $i_{Z,\text{max},\text{rated}}$ could be less than $P_{Z,\text{rated}}/V_Z$ if a safety factor is applied.

Finally, the required value for the filter capacitor $C$ is calculated. When all four rectifier diodes are reverse biased and the capacitor is discharging, we can make the conservative approximation that $i_S$ is close to its peak value at all times. Thus,

$$i_S = -C \frac{dv_C}{dt} \approx -C \left( -\frac{V_{\text{max}} - V_{\text{min}}}{0.5T} \right) = 2Cf(V_{\text{max}} - V_{\text{min}}) = 2CfV_r,$$

where $T$ and $f$ are the period and frequency, respectively, of the AC voltage driving the circuit (in the United States, $f = 60$ Hz). Substituting the relationship $V_r = 0.2(V_{\text{max}} - V_Z)$ into the expression for $i_S$ leads to

$$i_S = 2CfV_r = 2Cf(0.2(V_{\text{max}} - V_Z)) = 0.4Cf(V_{\text{max}} - V_Z),$$

from which we obtain

$$C_{\text{min}} = \frac{i_S}{0.4f(V_{\text{max}} - V_Z)}.$$  

With $i_S$ set to its maximum possible value,

$$i_{S,\text{max}} = \frac{V_{\text{max}} - V_Z}{R_S},$$

which yields

$$C_{\text{min}} = \frac{V_{\text{max}} - V_Z}{0.4f(V_{\text{max}} - V_Z)R_S} \rightarrow C_{\text{min}} = \frac{1}{0.4fR_S}.$$  

The capacitor value actually used should be the next standard value above the calculated minimum value.
Experimental Procedure

Warning #1: Do not attempt to measure both $v_{sec}$ and $v_o$ in Figure 2 with the oscilloscope at the same time. The ground leads could create a short between two circuit nodes that could destroy one of the diodes. You should inspect Figure 2 and understand how this can happen before proceeding.

Warning #2: Electrolytic capacitors are polarized. The marking on an electrolytic capacitor’s package usually indicates its negative terminal. Look for a thick “−” sign, and interpret chevrons (angled lines) as arrows.

- Design a regulated power supply like the one shown in Figure 2 using one of the supplied transformer boxes. The power supply should meet the following specifications:

  DC output voltage: approximately 9 V
  Maximum load current: 50 mA
  “Bleeder” resistance $R_b$: should discharge the capacitor to 5% of its maximum voltage within 5 seconds after the power supply is turned off; however, it should not load down the rectifier significantly when the power supply is on (i.e., it should not add significantly to $i_Z + i_L$).

Recommendations and hints:

1. Check the peak voltage of the transformer’s secondary (end-to-end and center-to-end).
2. The capacitor will discharge to the zener voltage $V_Z$ quickly even without the bleeder resistor $R_b$ in place. (Do you know why?) Select the value of $R_b$ to discharge $C$ the rest of the way to zero volts within a few seconds.
3. Measure or look up the turn-on voltage of the rectifier diodes you use. Consult the appropriate plot in the data sheet. Data sheets for standard pn-junction and zener diodes are available via links on the Laboratory web page.
4. Determine the expected dissipated power of all resistors and diodes (including $R_L$), and modify the design if necessary to avoid exceeding device ratings. It might be necessary to estimate the average values of the currents $i_S$ and/or $i_Z$; make sure your estimates are reasonable for the worst cases expected. Apply a $\times 1.5$ safety factor.
5. Electrolytic capacitors may be combined in series and/or parallel if capacitors of the desired standard value are not available. However, keep in mind the tolerances of the capacitors and the imprecision of the various rules of thumb employed in the design. Do not waste money by overdesigning.

- Devise a way to test whether or not your power supply is working correctly at full rated output current. A successful test includes ensuring that none of the components overheats and that the capacitor discharges within the specified period of time. Once you are confident that your circuit is working, demonstrate it to the instructor or TA.

- With the power supply delivering its maximum rated load current, capture a screen image of the output waveform $v_o$ and the capacitor voltage $v_C$ being simultaneously displayed. Also calculate the percentage ripple of the output voltage waveform. You might need to change the oscilloscope’s settings for the latter task in order to observe the tiny ripple voltage.
- Measure and record the DC output voltage obtained when the supply provides the maximum rated load current, half of the maximum load current, and no load current. Use the bench-top voltmeter in order to obtain measurements with several digits of accuracy. The three measured values should be slightly different. In your lab summary, explain your observations qualitatively by referring to the piecewise linear model for a zener diode operating in the reverse-breakdown region.

**Lab Summary**

After your group has completed the assigned tasks and demonstrated a working circuit, prepare a written summary no more than two pages long (not including the screen captures) that includes but is not necessarily limited to the following elements:

a. Description of all circuit design choices (including power dissipation calculations), assembly steps, and results of measurements with diagrams as appropriate.
b. Screen captures (with appropriate annotations and captions) of the capacitor and output voltage waveforms.
c. An explanation of why the output voltage changes as the load current varies.
d. A conclusion that discusses the implications of the results and of outcomes that are unexpected or at least not obvious (e.g., how realistic design constraints might have affected your ability to meet specifications). Point out ideas, relationships, impacts, implications, etc. that the reader might miss without your guidance.

The summary should follow the format specified in the previous lab handouts and the “Lab Summary Guidelines” posted at the Laboratory web page. The first page should include the group members’ names, the course number (ELEC 350), the lab section (Monday or Wednesday), the lab number, and the lab date (not the summary due date).

**Grading**

Each group member will receive the same grade based on the following criteria. Scores will be quantized at the indicated percentage levels.

<table>
<thead>
<tr>
<th>Percentage</th>
<th>Description</th>
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</thead>
<tbody>
<tr>
<td>0, 15, 30, 45, 60%</td>
<td>Demonstration of fully operational circuit that meets specifications</td>
</tr>
<tr>
<td>0, 5, 10, 15, 20%</td>
<td>Summary – Completeness and technical accuracy</td>
</tr>
<tr>
<td>0, 5, 10%</td>
<td>Summary – Organization, neatness, and style (professionalism)</td>
</tr>
<tr>
<td>0, 5, 10%</td>
<td>Summary – Spelling, grammar, and punctuation</td>
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As outlined in the lab policies and guidelines, any group member who misses any portion of the lab session and is not excused will receive a grade penalty proportional to the time absent.

If the demonstration is not completed by the end of the lab session, full demonstration credit can be obtained if the circuit is made to operate and a detailed one-page (or less) explanation of the problem and its solution is provided within 24 hours. The explanation is separate from the lab summary.
The lab summary is due at the beginning of next week’s lab session. Summaries submitted after the deadline but before 6 pm on the following day will result in a 20% grade deduction applied to the lab grade. No credit will be given for a summary submitted later, although credit for successful demonstration of the assigned circuit will still be given.

**Group Assignments**

The randomly generated groups for this lab exercise are listed below:

*Monday section*
- Hough-Daughan
- Kaspar-Rocci
- Ludwig-DAbbraccio
- Hontz-MacGibbon
- Gegg-Brown-Goesseringer

*Wednesday section*
- Carno-Bekampis
- Kwiatkowski-Ononuju
- Opalinski-Bacon
- Moore-Bennett
- Breen-Mylet
- Clark-Sommers

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