Introduction

Digital circuit design has emerged as an extremely important discipline in the modern technical world. All digital circuits, from simple combinational logic circuits to sophisticated computer processor chips such as those manufactured by Intel and AMD, employ logic gates that perform the basic Boolean functions such as AND, OR, NAND, NOR, etc. All of the basic logic gates are implemented in the major logic families. The CMOS (complementary metal-oxide semiconductor) family is currently the most widely used because of its low power dissipation properties and because of its high density of gates in integrated circuit (IC) chips. In this lab exercise you will analyze the operation of a basic CMOS logic gate and then verify your analysis via a test procedure of your own design.

Pre-Lab Work and Quiz

There will be no quiz or pre-lab work for this lab exercise, except to read over this handout carefully before the lab session. The more familiar you are with the task ahead, the more efficiently you will be able to use your lab time.

Theoretical Background

The most fundamental logic gate in any logic family is the NOT gate, or inverter. The output of a NOT gate is simply the complement of the input. That is, an input of 0 yields an output of 1, and vice versa. The other types of combinational logic gates, the AND, OR, NAND, NOR, XOR, and XNOR gates, have two or more inputs. For two-input gates with inputs labeled $A$ and $B$, the following truth table defines the output states for the indicated Boolean operations:

<table>
<thead>
<tr>
<th>Inputs</th>
<th>Boolean Operation</th>
</tr>
</thead>
<tbody>
<tr>
<td>$A$</td>
<td>$B$</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
</tr>
</tbody>
</table>

In the CMOS logic family, these Boolean operations are implemented on IC chips that contain both $p$-channel (PMOS) and $n$-channel (NMOS) MOSFETs. For enhancement-mode NMOS devices in normal operation, the drain current $i_D$, the drain-to-source voltage $v_{DS}$, the threshold voltage $V_{TH}$, and the transconductance parameter $k_n = \mu_n C_{ox} W/L$ are all positive quantities. The corresponding quantities for enhancement-mode PMOS devices, except the drain current and transconductance parameter, are negative. The gate-to-source voltage $v_{GS}$ for an enhancement-mode NMOS device is typically positive, so if $v_{GS} < V_{TH}$, then the NMOS device operates in the cutoff region, where $i_D = 0$. Conversely, the value of $v_{GS}$ for an enhancement-mode PMOS device is negative, and if $v_{GS} > V_{TP}$, where $V_{TP}$ has a negative value (i.e., if $|v_{GS}| < |V_{TP}|$), then the PMOS device operates in the cutoff region.
Typical $i$-$v$ characteristics for NMOS and PMOS devices are shown in Figure 1. In the case of the CMOS logic family, all NMOS devices have gate-to-source voltages of either 0 V or $V_{DD}$, and all PMOS devices have gate-to-source voltages of either 0 V or $-V_{DD}$. This implies that the operating point of each device lies either along the upper curve in one of the plots in Figure 1 or along the horizontal axis. Note that the $|v_{GS}| = V_{DD}$ curve and the $v_{GS} = 0$ “curve” (the horizontal axis) in each plot intersect at the origin.

**Figure 1.** Graphical representations of the $i$-$v$ characteristics for $n$-channel and $p$-channel MOSFETs.

**Experimental Procedure**

You will be given a circuit diagram for a CMOS logic gate that implements an unknown (to you) Boolean operation. The power supply voltage for the circuit should be +10 V and is represented by the voltage bus labeled $V_{DD}$ in the diagram. Your assignment is to:

- Using circuit analysis, fill in the truth table for the circuit and determine which Boolean operation (NOT, AND, OR, NAND, NOR, XOR, or XNOR) the circuit implements.

To do this, you will need to describe the circuit’s operation for each of the four possible input states. That is, explain why the output is a logical 1 or 0 for a given set of inputs. Your explanation should include an accounting of which (if any) transistors are in the cutoff region, which (if any) are in the triode region, and which (if any) are in the saturation, or constant current, region. The implications of each transistor’s state should also be discussed. That is, explain which state(s) is characterized by a low resistance between the drain-source terminals of the transistor (and why), which state(s) leads to essentially zero current flow from drain to source (and why), and so forth.

You will find that determining the operating region of the one of the MOSFETs will be more challenging than for the other three, and you might find it impossible to determine the operating region of that MOSFET for one of the four input ($A$ and $B$) combinations. However, you should also be able to show that in that case it does not matter what the operating region of the MOSFET is.
- Warning: Do not apply input signals to a CD4007 until power ($V_{DD}$) has been applied to the circuit; otherwise, damage to the IC could result.

Pin 7 (the NMOS substrate) must be connected to ground and pin 14 (the PMOS substrate) must be connected to $V_{DD}$ regardless of the circuit configuration of the IC.

Confirm your analysis in the preceding step by building the logic gate using a CD4007 chip and then designing a test procedure to determine the gate’s truth table. Remember to record important details such as which transistors on the chip correspond to the transistors in the circuit (e.g., specify pin numbers next to the transistor terminals in your circuit diagram), and describe the test configuration that you used, including how you supplied a logical 0 or 1 to each gate input and how you determined the output level.

Figure 2 shows the pin-out of the CD4007 chip. Note that the pins in the diagram are not in numerical order. The substrates of the three NMOS devices are connected together at pin 7, and the substrates of the three PMOS devices are connected together at pin 14. One PMOS device and one NMOS device each have their sources connected internally to their respective substrates. The sources of the other transistors must be connected to their respective substrates externally, if the design calls for that. One NMOS-PMOS pair (pins 9-12) is already configured as a CMOS inverter; that is, their gates and drains are connected together internally. You might be able to take advantage of the inverter configuration when you construct your circuit.

A data sheet for the CD4007 is available via a link on the Laboratory web site.

Figure 2. Pin-out of the CD4007 dual complementary pair plus inverter.

- Demonstrate your working logic gate to the lab instructor.

- For your report, prepare a table showing the operating region of each transistor in your logic gate for each of the four possible binary input combinations.
Grading

Each group must submit a brief but well written report that describes in detail all circuit design choices, assembly steps, test configurations, and the results of measurements. The report should include (but not necessarily be limited to) all of the details requested in the “Experimental Procedure” section. As explained below, the identification of the MOSFETs’ operating regions will be assigned a separate grade from the “Completeness and technical accuracy” portion.

The report is due at the beginning of next week’s lab session. Each group member will receive the same grade, which will be determined as follows:

30% Properly operating logic circuit
20% Proper identification of operating region for each MOSFET for each input state (in the report; separate grade for this item)
30% Report – Completeness and technical accuracy
10% Report – Organization, neatness, and style (professionalism)
10% Report – Spelling, grammar, and punctuation

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