Successful completion of the following exercise will result in 5 points being added to your lab group’s average lab grade for the semester. The points will not be added to the individual writing assessment grade under any circumstances.

Assignment:

Design and assemble a four-resistor bias network like the one shown in Fig. 6.60a of the textbook for a 2N3904 bipolar junction transistor using either the biasing method described in the textbook or the alternative method described in class. The target specifications are:

\[
\begin{align*}
V_{CC} &= 15 \text{ V (power supply voltage)} \\
V_C &= 10 \text{ V (quiescent voltage at the collector node)} \\
I_C &= 10 \text{ ma (quiescent collector current)} \\
\text{Max. power dissipation of any single resistor} &< 125 \text{ mW (resistors are rated at 250 mW)}
\end{align*}
\]

Note that these specifications are the same as the ones given in one of your homework problems. If you need a value for the \( \beta \) parameter of the BJT, deduce it from the information given in the 2N3904 data sheet, which is available via a link on the Laboratory web page. Use the closest standard 5% resistor values for all four resistors in the network. You may use multiple resistors to implement a single resistance value only if necessary to meet power dissipation requirements.

After the design is finished, assemble and test the circuit, and then arrange a time to demonstrate it. You must show that the measured collector voltage (and by extension, the collector current) is close to the specified quiescent value and moves little from that point when the circuit is heated using a hair dryer. You must also show a brief (one page or less) and legible set of calculations for arriving at each resistor value.

Demonstrations may take place during my office hours or at another arranged time. They may take place during the Reading Day (Wednesday, December 5) only if specifically requested by your group. Some demonstration times might be available over the weekend of December 1-2. No demonstrations may take place after December 5.

Notes:

1. A supply of 2N3904 transistors is available in the gray bins in Dana 303.
2. No assistance will be provided for the demonstrations. You must interpret the data sheet, debug any circuit wiring problems, tame any spurious oscillations, and work around other issues on your own.
3. Your group must work alone. You are on your honor not to share any design approaches with other groups.
4. No partial credit will be given for a circuit that does not meet the full specifications, including meeting power dissipation limits. This is an “all-or-nothing” opportunity.
5. Only one demonstration per group will be allowed. You must ensure that your circuit works properly before the demonstration begins. A circuit that works properly at first and then fails during the demonstration will be considered nonfunctional and will result in no extra credit.