Policies and Review Sheet for Exam #2

The following policies will be in effect for the exam. They will be included in a list of instructions and policies on the first page of the exam:

1. You will be allowed to use a non-wireless enabled calculator, such as a TI-89.
2. You will be allowed to use two 8.5 × 11-inch two-sided handwritten help sheets. No photocopied material or copied and pasted text or images are allowed. If there is a table or image from the textbook or some other source that you feel would be helpful during the exam and that is not included on the table and formula sheet that I will provide, please notify me.
3. All help sheets will be collected at the end of the exam but will be returned to you later.
4. If you begin the exam after the start time, you must complete it in the remaining allotted time. However, you may not take the exam if you arrive after the first student has completed it and left the room. The latter case is equivalent to missing the exam.
5. **You may not leave the exam room without prior permission except in an emergency or for an urgent medical condition. Please use the restroom before the exam.**

The exam will take place 8:00–9:50 am on Thursday, March 21 in Breakiron 065.

The following is a list of topics that could appear in one form or another on the exam. Not all of these topics will be covered, and it is possible that an exam problem could cover a detail not specifically listed here. However, this list has been made as comprehensive as possible. **You should be familiar with the topics on the review sheet for the previous exam as well.**

Although significant effort has been made to ensure that there are no errors in this review sheet, some might nevertheless appear. The textbook and the supplemental readings are the final authority in all factual matters, unless errors have been specifically identified there. You are ultimately responsible for obtaining accurate information when preparing for the exam.

Current mirrors in general

- significance of matching BJTs (or MOSFETs)
- need for diode-connected configuration in reference path of mirror
- characteristics of a “good” current source
- calculation of Norton equivalent resistance using a test source (analysis)
- calculation of Norton equivalent circuit via measured I_L or V_L vs. R_L data
- current steering: ability to bias multiple amplifiers from one reference branch
- one mirror can serve as the current reference for another mirror
- current sink (usually NPN or NMOS) vs. current source (usually PNP or PMOS)
- output current variation vs. output voltage variation (i.e., I_L varies as R_L varies)
- concept of compliance limit
- mirrors can serve as active loads in amplifiers; if so, then equivalent small-signal resistance of active load = output resistance of mirror

MOSFET current mirror

- only functions properly when MOSFETs are in saturation region (not cut-off or triode)
- calculation of resistor value in reference circuit branch
- can make output current I_O different from reference current I_{REF} by using different channel widths
- simple mirror circuit (one MOSFET in reference branch and one in "pass" branch)
    - compliance voltage is V_{OV} (= $V_{GS} - V_t$) of pass transistor
    - output (Norton equiv.) resistance is r_o of MOSFET (i.e., equal to V_A/I_D)
    - current transfer ratio: $\frac{I_O}{I_{REF}} = \frac{W_2/L_2}{W_1/L_1}\left(1 + \frac{V_{DS2} - V_{GS2}}{V_{A2}}\right)$, where Q_1 is reference transistor, Q_2 is output ("pass") transistor; factor in parentheses accounts for effect of r_{o2} (transfer ratio is for NMOS; modify slightly for PMOS)
- Wilson mirror circuit
    - compliance voltage is $V_{t1} + V_{OV3}$, where Q_1 is diode-connected transistor and Q_3 is output (pass) transistor (next to load)
    - output resistance is approx. $g_{m3}r_{o3}r_{o2}$, where Q_2 is transistor in reference leg and Q_3 is output transistor (next to load)

BJT current mirror

- only functions properly when BJTs are in active region (not cut-off or saturation)
- calculation of resistor value in reference circuit branch
- can make output current I_O different from reference current I_{REF} by using different base-emitter junction areas (scale current I_S is directly proportional to area)
- scale current: $I_S = \frac{A_E q D_n n_i^2}{N_A W}$, where

  A_E = cross-sectional area of base-emitter junction (cm^2)
  q = magnitude of electron charge (1.6×10^{-19} C)
  D_n = electron diffusivity in the base (~35 cm^2/s in Si)
  n_i = intrinsic carrier density (cm^{-3})
  N_A = doping concentration of acceptor ions (cm^{-3})
  W = effective width of the base (cm)
- simple mirror circuit (one BJT in reference branch and one in "pass" branch)
    - compliance limit is approx. 0.3 V ($V_{CE}|_{sat}$ of output or pass transistor)
    - output (Norton equiv.) resistance is r_o of BJT (i.e., equal to V_A/I_C)
    - current transfer ratio: $\frac{I_O}{I_{REF}} = \frac{1}{1 + \frac{2}{\beta}}\left(1 + \frac{V_{CE2} - V_{BE}}{V_{A2}}\right)$, where "2" subscript refers to output ("pass") transistor; factor in parentheses accounts for effect of r_{o2} (transfer ratio is for *npn*; modify slightly for *pnp*)
- Wilson mirror circuit
    - compliance limit is approx. 1 V ($V_{CE}|_{sat} + V_{BE}$)
    - output resistance is approx. $\beta r_o/2$, where Q_2 is output transistor (next to load)
    - current transfer ratio: $\frac{I_O}{I_{REF}} = \frac{1}{1 + \frac{2}{\beta^2}}$, if effect of r_o is neglected

- Widlar mirror circuit
  - Like simple mirror circuit, except that a resistor R_E is added in series with the emitter of the "pass" BJT
  - current transfer relationship (transcendental equation):

    $I_O R_E = V_T \ln\left(\frac{I_{REF}}{I_O}\right)$, if effect of r_o is neglected
  - compliance voltage is $V_{CE}|_{sat} + V_{RE}$, where V_{RE} is the voltage across the emitter resistance R_E that is in series with the "pass" BJT; V_{RE} is typically ~0.1 V or less
  - typically, $I_{REF} >> I_O$, so both R_{REF} and R_E are reasonable in size for IC chips (both a few kilohms or smaller)
  - output resistance: $R_{out} \approx \left[1 + g_{m2}\left(R_E \| r_{\pi 2}\right)\right] r_{o2}$,

    where Q_2 is the "pass" or output transistor (in series with load); for typical values of V_{RE} (voltage across R_E), about 0.2 V or less, this can also be expressed as

    $R_{EE} \approx \left(1 + \frac{V_{RE}}{\eta V_T}\right) r_{o2}$
  - advantages are high output resistance (although roughly an order of magnitude less than that of a Wilson mirror) with low compliance limit (comparable to simple mirror) and small resistors on IC chip

Differential amplifiers ("diff amps")

- concept of differential-mode and common-mode signal voltages (v_{id}, v_{od}, and v_{icm})
- input voltage v_{in} could be differential-mode, common-mode, or both (superposition)
- $v_{id} = v_{IN1} - v_{IN2}$, $v_{od} = v_{o2} - v_{o1}$ (or $v_{o1} - v_{o2}$), and $v_{icm} = \frac{v_{IN1} + v_{IN2}}{2}$

  but remember that common-mode voltage could also have a bias (quiescent) component; the bias component is not a signal
- concept of a differential (or "floating") voltage vs. a "single-ended" voltage (voltage measured relative to reference node)
- common-mode rejection ratio (CMRR) for differential-mode output: $\text{CMRR} = \frac{|A_d|}{|A_{cm}|}$
- expression of CMRR in dB

  $\text{CMRR[dB]} = 20\log\frac{|A_d|}{|A_{cm}|}$; "20" is used b/c CMRR is based on voltage gains
- major advantages of diff-amps:
  - bypass capacitor for MOSFET source degeneration resistor or BJT emitter degeneration resistor not needed
  - reduced number of large capacitors needed
  - consist completely (or almost completely) of transistors; few/no resistors needed
  - with care, can provide substantial gain down to zero frequency (DC)
  - rejection of common-mode signals

Differential amplifiers based on BJTs

- for **purely** differential-mode inputs, $v_e \approx 0$ (i.e., the signal component of the node voltage at the emitters of the two amplifying BJTs is essentially zero); there is essentially a virtual small-signal ground at the emitter terminals
- virtual ground does **not** exist at emitter terminals of amplifying BJTs for common-mode inputs

- input common-mode range (for bias only)

  $V_{CM\max} \approx V_C + 0.4 = V_{CC} - \alpha \frac{I_O}{2} R_C + 0.4$ and $V_{CM\min} = -V_{EE} + V_{comp} + V_{BE}$,

  where V_{CC} and V_{EE} (neg. value) are pos./neg. power supply voltages; V_{comp} = compliance limit of current mirror; V_{BE} = forward voltage drop of base-emitter junction (usually 0.7 V); R_C = collector resistances; $\alpha = \beta/(\beta+1)$; and 0.4 V = $V_{BE} - V_{CE}|_{\text{sat}}$ = 0.7 V – 0.3 V. Note: This ignores the presence of a differential-mode signal; these relationships are only for bias conditions.
- all BJTs must operate in the active region (i.e., avoid cut-off and saturation)
- large-signal operation: total (bias + signal) emitter currents are given by

  $i_{E1} = \frac{I_O}{1 + e^{-v_{id}/\eta V_T}}$ and $i_{E2} = \frac{I_O}{1 + e^{v_{id}/\eta V_T}}$

  where $v_{id} = v_{IN1} - v_{IN2}$; I_O = current mirror value; η = emission coef. (value is 1 to 2); V_T = thermal voltage (about 25 mV at room temp.)
- if $|v_{id}| > \sim 4\eta V_T$ (about 100 mV at room temperature), then I_O will flow almost entirely on one side of diff amp
- small-signal condition: limit on input voltage applied to diff amp to avoid nonlinearity ($|v_{id}| << 2\eta V_T$, although $|v_{id}|$ can be a little higher in many practical cases)
- in a diff amp with single-ended input, the BJT with the grounded base acts as an emitter bypass device for signals for the driven BJT; this avoids the need for a bypass capacitor at the emitter, unlike a simple common-emitter amplifier; the bypassing is effective at very low frequencies and at DC
- equivalent resistance of BJT looking into emitter (equals $r_e = \alpha/g_m \approx 1/g_m$)
- voltage gain expressions (valid for $R_L \to \infty$):
  - differential or single-ended input, single-ended output

    $A_{d,se1} = \frac{v_{o1}}{v_{id}} = -\frac{1}{2} g_m R_C$ and $A_{d,se2} = \frac{v_{o2}}{v_{id}} = +\frac{1}{2} g_m R_C$;

    where $g_m = \frac{I_C}{\eta V_T} = \frac{I_O}{2\eta V_T}$ and $v_{id} = v_{IN1} - v_{IN2}$;

    for greater accuracy, replace R_C with $R_C||r_o$, where r_o is for Q_1 and Q_2
  - differential or single-ended input, differential output

    $A_{d,d} = \frac{v_{od}}{v_{id}} = g_m R_C$;

    for greater accuracy, replace R_C with $R_C||r_o$, where r_o is for Q_1 and Q_2
  - common-mode input, single-ended output

    $A_{cm,se1} = \frac{v_{o1}}{v_{icm}} = A_{cm,se2} = \frac{v_{o2}}{v_{icm}} = -\frac{\alpha R_C}{r_e + 2R_{EE}} \approx -\frac{R_C}{2R_{EE}}$,

    where R_{EE} = Norton equiv. resistance of current mirror; good approximation for matched or mismatched BJTs and/or resistors; for greater accuracy, replace R_C with $R_C||r_o$, where r_o is for Q_1 and Q_2
  - common-mode input, differential output

    $A_{cm,d} = \frac{v_{od}}{v_{icm}} = 0$, if BJTs and resistors are matched

    $A_{cm,d} = \frac{v_{od}}{v_{icm}} \approx -\left(\frac{R_C}{2R_{EE}}\right)\left(\frac{\Delta g_m}{g_m} + \frac{\Delta R_C}{R_C}\right)$, for mismatched BJTs and resistors; for greater accuracy, replace R_C with $R_C||r_o$,

- effect of finite single-ended load resistance on single-ended gain and on quiescent collector voltages
- input resistances:
  - differential-mode: $R_{id} = 2r_\pi$
  - common-mode: $R_{icm} = \beta R_{EE} \dfrac{1+\dfrac{R_C}{\beta r_o}}{1+\dfrac{R_C+2R_{EE}}{r_o}}$

Differential amplifiers based on BJTs with PNP mirror loads

- no resistors required (except possibly in current mirror and/or to mitigate input offset voltage)
- Q_1 and Q_2 (amplifying BJTs) are matched
- Q_3 and Q_4 (current mirror active loads) are matched; one is diode-connected
- can be used for single-ended output only
- the differential-mode input, single-ended output gain is $A_d \approx g_{m1}\left(r_{o1} \| r_{o3}\right)$ for infinite load ($R_L \to \infty$), where the output is taken from the collector of Q_1 and Q_3 is the corresponding active load on that side; gain is often reduced substantially for finite R_L
- current sourced or sunk at output terminal is limited to mirror current I_{EE}; this is the cause of slew rate limiting if following amplifier stage has a compensation capacitor

Differential amplifiers based on MOSFETs [THIS TOPIC IS NOT ON EXAM; THIS IS FOR INFORMATION ONLY]

- for differential-mode inputs, $v_s \approx 0$ (node voltage at source terminals of amplifying MOSFETS); virtual small-signal ground at source terminals
- virtual ground does **not** exist at source terminals of amplifying MOSFETs for common-mode inputs
- equiv. resistance looking into MOSFET's source terminal (relative to ground) is $r_s = 1/g_m$
- input common-mode range (for bias only)

  $V_{CM\max} = V_{DD} - \dfrac{I_O}{2} R_D + V_t$ and $V_{CM\min} = V_{SS} + V_{comp} + V_{OV} + V_t$,

  where V_{DD} and V_{SS} (neg. value) are pos./neg. power supply voltages; V_{comp} = compliance limit of current mirror; V_{OV} = overvoltage ($V_{GS} - V_t$) of amplifying FETs; and R_D = drain resistances. Note: This ignores the presence of a differential-mode signal; these relationships are only for bias conditions.
- all MOSFETs must operate in the saturation region (i.e., avoid cut-off and triode)
- large-signal operation: total (bias + signal) drain currents are given by

  $i_{D1} = \dfrac{I_O}{2} + \left(\dfrac{I_O}{V_{OV}}\right)\left(\dfrac{v_{id}}{2}\right)\sqrt{1-\left(\dfrac{v_{id}}{2V_{OV}}\right)^2}$ and $i_{D2} = \dfrac{I_O}{2} - \left(\dfrac{I_O}{V_{OV}}\right)\left(\dfrac{v_{id}}{2}\right)\sqrt{1-\left(\dfrac{v_{id}}{2V_{OV}}\right)^2}$

  where I_O = mirror current; this is valid for $-\sqrt{2}V_{OV} \le v_{id} \le \sqrt{2}V_{OV}$
- small-signal approximation (if $v_{id} << 2V_{OV}$):

  $i_{D1} = I_{D1} + i_{d1} \approx \dfrac{I_O}{2} + \left(\dfrac{I_O}{V_{OV}}\right)\left(\dfrac{v_{id}}{2}\right) \quad \to \quad i_{d1} \approx \dfrac{I_O}{2V_{OV}} v_{id} = \dfrac{1}{2} g_m v_{id}$

- voltage gain expressions (valid for $R_L \to \infty$):
  - differential or single-ended input, single-ended output

    $A_{d,se1} = \frac{v_{o1}}{v_{id}} = -\frac{1}{2} g_m R_D$ and $A_{d,se2} = \frac{v_{o2}}{v_{id}} = +\frac{1}{2} g_m R_D$,

    where $g_m = \frac{2I_D}{V_{OV}} = \frac{2(I_O/2)}{V_{OV}} = \frac{I_O}{V_{OV}} = \sqrt{2k_n I_D} = \sqrt{k_n I_O}$ and $v_{id} = v_{IN1} - v_{IN2}$;

    for greater accuracy, replace R_D with $R_D \| r_o$, where r_o is for Q_1 and Q_2
  - differential or single-ended input, differential output

    $A_{d,d} = \frac{v_{od}}{v_{id}} = g_m R_D$; where $v_{od} = v_{o2} - v_{o1}$;

    for greater accuracy, replace R_D with $R_D \| r_o$
  - common-mode input, single-ended output

    $A_{cm,se1} = \frac{v_{o1}}{v_{icm}} = A_{cm,se2} = \frac{v_{o2}}{v_{icm}} = -\frac{R_D}{1/g_m + 2R_{SS}} \approx -\frac{R_D}{2R_{SS}}$,

    where R_{SS} = Norton equiv. resistance of current mirror
  - common-mode input, differential output

    $A_{cm,d} = \frac{v_{od}}{v_{icm}} = 0$, if MOSFETs and resistors are matched

    $A_{cm.d} \approx -\left(\frac{R_D}{2R_{SS}}\right)\left(\frac{\Delta g_m}{g_m} + \frac{\Delta R_D}{R_D}\right)$, if resistors and/or g_m values are not matched
- effect of finite single-ended (s.e.) load resistance on s.e. gain & quiescent drain voltage
- CMOS diff amp with PMOS mirror loads
  - no resistors required
  - no body effect in PMOS active loads (sources can be tied to substrates)
  - Q_1 and Q_2 (amplifying MOSFETs) are matched
  - Q_3 and Q_4 (current mirror active loads) are matched; one is diode-connected
  - output is single-ended only
  - the differential-mode input, single-ended output gain is $A_d \approx g_{m1}(r_{o1} \| r_{o3})$, where Q_1 is the amplifying device on one side, and Q_3 is the corresponding active load on that side

Input offset voltages in diff amps

- BJTs:
  - input offset voltage due to resistor mismatch: $|V_{OS}| = nV_T\left(\frac{\Delta R_C}{R_C}\right)$
  - input offset voltage due to base-emitter junction area mismatch:

    $|V_{OS}| = nV_T\left(\frac{\Delta I_S}{I_S}\right) = nV_T\left(\frac{\Delta g_m}{g_m}\right)$,

    where I_S = scale or saturation current $\left(\text{from } I_C = I_S e^{v_{BE}/nV_T}\right)$
  - for current mirror loads, input offset voltage due to error in current transfer ratio caused by finite β_L of load BJTs (could be *pnp* or *npn*):

    $V_{OS} \approx -\frac{2nV_T}{\beta_L}$
  - in practice, multiple mismatches are simultaneously present

- MOSFETs: [NOT ON EXAM; FOR INFORMATION ONLY]
  - input offset voltage due to resistor mismatch: $|V_{OS}| = \frac{V_{OV}}{2}\left(\frac{\Delta R_D}{R_D}\right)$
  - input offset voltage due to W/L mismatch: $|V_{OS}| = \frac{V_{OV}}{2}\left[\frac{\Delta(W/L)}{W/L}\right]$, where W = width of channel; L = length
  - input offset voltage due to threshold voltage mismatch: $|V_{OS}| = \Delta V_t$
  - in practice, multiple mismatches are simultaneously present

Relevant course material:

HW: #4, #5, and #6
Labs: #3
Reading: Assignments from Feb. 10 through Mar. 6, including the supplemental readings
"Norton Equivalent Circuits of Current Mirrors"
"Widlar Current Source"

This exam will focus primarily on the course outcomes list below and related topics such as biasing:

2. Analyze and design basic current mirror circuits.
3. Analyze the differential-mode and common-mode characteristics of BJT and MOSFET-based differential amplifiers. [only BJT diff amps on Exam #2]

The course outcomes are listed on the Course Policies and Information sheet, which was distributed at the beginning of the semester and is available on the Syllabus and Policies page at the course web site. The outcomes are also listed on the Course Description page. Note, however, that some topics not directly related to the course outcomes could be covered on the exam as well.