Please review the “Exam Policies” section of the Exams page at the course web site. Please note the following two changes from policies used in the past:

1. You will be allowed to use one 8.5 × 11-inch two-sided handwritten help sheet. No photocopied material or copied and pasted text or images are allowed. If there is a table or image from the textbook or some other source that you feel would be helpful during the exam, please notify the instructor.
2. All help sheets will be collected at the end of the exam but will be returned to you later.

The following is a list of topics that could appear in one form or another on the exam. Not all of these topics will be covered, and it is possible that an exam problem could cover a detail not specifically listed here. However, this list has been made as comprehensive as possible.

Although every effort has been made to ensure that there are no errors in this review sheet, some might nevertheless appear. The textbook is the final authority in all factual matters, unless errors have been specifically identified there. You are ultimately responsible for obtaining accurate information when preparing for your exam.

General small-signal modeling
- definition of “incremental signal”
- separation of bias considerations (quiescent levels; output voltage swing range) from small-signal considerations (gain, input and output resistance)
- replacement of DC voltage sources with short circuits (because the voltage across a DC voltage source cannot change with time)
- replacement of DC current sources with open circuits (because the current through a DC current source cannot change with time)
- why DC voltage sources are typically bypassed at AC (i.e., at signal frequency) using capacitors
- small-signal model of BJT is valid only when device operates in the active region but not in cut-off or saturation regions
- small-signal model of FET is valid only when device operates in the saturation region but not in cut-off or triode regions
- derivation of small-signal voltage gain
- difference between open-circuit gain $A_{vo}$, amplifier gain $A_v$, and overall gain $G_v$
- derivation of small-signal input resistance $R_{in}$
- derivation of small-signal output resistance $R_o$
- simplifications in gain/resistance expressions when one term is much greater/smaller than another term
- derivation of the input or output resistance “looking into” a particular pair of terminals using a test source ($v_t$ and $i_t$)

Two-port amplifier representation
- $v_{in}$ and $v_o$ are the voltages measured at the amplifier’s input and output terminals
- a set of input or output terminals is sometimes called a “port”
- input port of amplifier has an equivalent input resistance $R_{in}$
- $A_v =$ voltage gain with load; $A_{vo} =$ “open-circuit” voltage gain ($R_L \to \infty$)
- output port of amplifier can be represented as a Thévenin equivalent circuit with voltage source $A_{vo}V_{in}$ and output resistance $R_o$
- relationship between source resistance $R_{s0}$ and input resistance $R_{in}$ required to maximize input voltage or current to amplifier
- relationship between output resistance $R_o$ and load resistance $R_L$ required to maximize output voltage or current from amplifier

Small-signal modeling of BJT circuits
- small-signal models of BJT: hybrid-pi model and T model
- small-signal condition: $V_{be} \ll nV_T,$ where $n =$ emission coefficient (usually assumed to equal unity); and $V_T =$ thermal voltage, related to temperature $T$ in kelvins by $V_T = T/11,600$
- incremental base-emitter resistance $r_\pi$ and what it represents (finite slope of $i_B-V_{BE}$ characteristic of base-emitter $pn$-junction, which obeys diode equation):
  \[ r_\pi = \frac{nV_T}{I_B} = \frac{\beta}{g_m} = r_e(\beta + 1) \]
- incremental collector-emitter resistance $r_o$ (called transistor output resistance in the textbook) and what it represents (non-zero slope of $i_C-V_{CE}$ characteristic in the active region); typically 50 kΩ or more for BJTs
- relationship between small-signal output port resistance (collector-emitter resistance) and Early voltage ($V_A$):
  \[ r_o \approx \frac{V_A}{I_C} \]
- dependence of $g_m$ of BJT on quiescent collector current $I_C$:
  \[ g_m = \frac{I_C}{nV_T} \]
- relationship between $\alpha$ and $\beta$ (where $I_C = \alpha I_E$):
  \[ \alpha = \frac{\beta}{\beta + 1} \]
- emitter resistance $r_e$ in T model of BJT:
  \[ r_e = \frac{\alpha}{g_m} = \frac{r_\pi}{\beta + 1} \]
- derivation of $g_m$ from $i_C$ vs. $v_{BE}$ equation (diode eqn applied to BE junction)
- effect of emitter degeneration resistor ($R_E$) on gain, input resistance
- effect of “amount of negative feedback” ($1 + g_mR_E$) on peak allowable input voltage in CE amplifiers with emitter degeneration and its derivation
- typical values of important BJT and circuit parameters such as $\beta$, $r_o$, bias resistor values, and saturation voltage
- $pnp$ small-signal model: directions of $i_b$ and $\beta i_b$ and polarity of $v_{be}$ same as for $npn$ model
- data sheet notation: $h_{FE} = \beta; h_{fe} = \beta; h_{ie} = r_\pi; h_{oe} = r_o$

Small-signal modeling of MOSFET circuits
- small-signal models of MOSFET: hybrid-pi model and T model
- small-signal condition: $v_{gs} \ll 2V_{OV},$
  where $V_{OV} =$ bias overvoltage, which equals $V_{GS} – V_t$, where $V_{GS}$ is the quiescent gate-to-source voltage, and $V_t$ is the MOSFET’s gate threshold voltage
- gate-source path modeled as an open circuit in hybrid-pi model
- incremental drain-source resistance \( r_o \) (called transistor output resistance in the textbook) and what it represents (non-zero slope of \( i_D-v_{DS} \) characteristic in the saturation region); typically 20-60 kΩ for Si MOSFETs
- relationship of small-signal output port resistance (drain-source resistance) to Early voltage \( (V_A) \):
\[
r_o \approx \frac{V_A}{I_D}
\]
- small-signal gate-to-source resistance in T model simply labeled \( 1/g_m \) (could call it \( r_{gs} \) or \( r_s \) in an analogy to \( r_c \) for BJTs)
- typical values of important MOSFET and circuit parameters such as \( k_n \) (and \( k_p \)), \( V_t \), \( r_o \), and bias resistor values
- derivation of \( g_m \) from \( i_D \) vs. \( v_{GS} \) equation
- dependence of \( g_m \) of MOSFET on quiescent drain current \( I_D \)
\[
g_m = \sqrt{2k_nI_D} = \frac{2I_D}{V_{OV}},
\]
where \( k_n \) = device transconductance parameter, usually in mA/V² (labeled \( k_n \) for NMOS devices and \( k_p \) for PMOS devices)
- effect of source degeneration resistor \( (R_s) \) on gain
- effect of “amount of negative feedback” \( (1 + g_mR_s) \) on peak allowable input voltage in CS amplifiers with source degeneration and its derivation
- PMOS small-signal model: direction of \( g_mv_{gs} \) and polarity of \( v_{gs} \) same as for NMOS model

Basic amplifier design
- identify most restrictive specifications
- use analysis to derive relationships between component and device parameters (i.e., quantities like \( \beta \) and resistor values) and specified performance requirements such as gain and input/output resistance
- design bias network to adjust \( g_m \), swing range, and other parameters to satisfy specifications
- select capacitor values, bypass arrangements, etc.) to meet remaining specifications or to confirm that minimum performance requirements will be met

Note: If your understanding of BJT biasing and basics of operation is a bit weak, you should consult the review sheet for the ELEC 350 final exam from last semester. Consult the lecture notes on MOSFET biasing if your knowledge of that subject is a bit weak.

Relevant course material:
HW: #1, #2, #3
Labs: #1
Textbook: Sections 5.5.2, 5.5.7, 5.6.4, and 5.8 (except 5.8.6)
Sections 6.5 through 6.8 (except 6.8.6)
Lecture notes: Source Degeneration Biasing for Discrete MOSFET Amplifiers
Web Links: (none)
Mathcad: (none)
Matlab: (none)