Lab #1: BJT Bias Network Design

Introduction

Biasing is the process of selecting component values in an amplifier circuit so that the proper quiescent voltages and currents are established to meet a set of design goals. A frequent requirement is to keep the quiescent voltages and currents close to target values despite variations in device parameters. In other situations, the exact values of the voltages and currents are not so important, but their stability relative to temperature changes or other environmental variations *is* important. In this one-week lab exercise you will design, test, and compare two bias circuits for an *npn* BJT. Lab group assignments are listed at the end of this handout. Section 7.4.2 of the textbook (Sedra & Smith, 8th ed.) contains helpful guidance for this lab exercise.

Experimental Procedure

- Design a bias circuit like the one shown in Figure 1a for a 2N3904 npn BJT (i.e., find values for R_C, R_E, R_1, and R_2) to meet the following specifications:

  V_{CC} = 15 V I_C = 3.2 mA V_C = 2/3 of V_{CC}

  The values of I_C and V_C that you actually measure must be within 15% of the specified values. Select a reasonable value for the quiescent voltage across R_E given that this circuit is likely to be the starting point for an amplifier and that the BJT must stay out of the saturation region. Consult the 2N3904 data sheet at the course Laboratory web page for any information that you need about the transistor. Be sure to incorporate the constraints listed at the top of the next page.

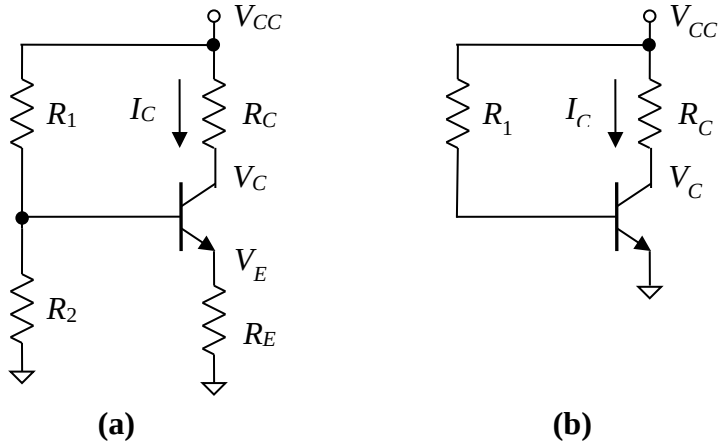

Figure 1. BJT biasing circuits (a) with and (b) without an emitter degeneration resistor.

Keep careful records of your bias design process and test procedure since you will need to explain and justify them as part of your post-lab work.

Your bias network design must satisfy the following additional constraints:

1. Select values for the base biasing resistors R_1 and R_2 that represent a reasonable compromise between bias stability and current demand from the power supply.
2. Ensure that the power dissipation limits of the BJT and resistors are not exceeded. Assume that all resistors have a 1/4 W maximum rating.
3. Use only one physical resistor for each resistance in the circuit unless multiple resistors are necessary to avoid exceeding power dissipation limits. In the latter case, each resistor in a series or parallel combination must have the same value. Each resistor used (either alone or in combination) must have a standard value in the E24 (5% tolerance) series.
4. You may use Multisim or other circuit analysis software to simulate your design before you assemble the actual circuit. However, remember that all aspects of the final design must be based on a deterministic process and not trial-and-error.

- Design a two-resistor bias circuit like the one shown in Figure 1b for the same I_C and V_C values and relevant constraints as those for the four-resistor bias circuit. Calculate a ballpark value for R_1, but note that you will probably have to adjust it to meet the specifications. You should therefore consider using a potentiometer, perhaps in series with a fixed resistor, to implement R_1. Trial-and-error is acceptable for finding a value for R_1. As in the previous circuit, check that none of the power dissipation ratings is exceeded. Carefully record your design process for your review and to support your post-lab work.

- Assemble both bias circuits on a protoboard using two different 2N3904 BJTs. Adjust the value of R_1 in the two-resistor circuit until the collector voltage is within 10% or so of its target value. A trial-and-error approach is acceptable. Record the measured quiescent collector voltage V_C for each circuit. The value for the two-resistor circuit might be rather unstable; that is okay. You only need to measure V_C since I_C is directly related to it. (Why?)

- Warm the BJT in each bias circuit using a hair dryer or by grasping it with your fingers until the value of V_C stabilizes. Record the new measured V_C value at the higher temperature. Be prepared to compare and explain qualitatively the difference in the temperature stability of the two bias networks. Record any important observations, including possible changes in the region of operation of the BJT.

- Compile the following data and visual aids so that you can easily refer to them during your post-lab meeting. The items may be handwritten or hand-drawn, but they must be legible and well organized with no extraneous notes or information.

    - brief outline of the design process for each bias network
    - diagrams of both bias circuits with component values clearly indicated (pay attention to how the potentiometer – if you used one – is represented)
    - measured collector voltages for both bias circuits at room and elevated temperatures
    - any observations or troublesome issues noted during the experiment

  Combine all of the visual aids that your group intends to use into a single PDF document and **e-mail** it to me before the post-lab meeting begins. The file name format should have the form:

"LName1_LName2_LName3_Lab1_sp24.pdf"

Add "LName4" if your group has four members. **The file size must be less than 5 MB.** Keep a copy of your documentation if you wish to use it to prepare for the next exam or need it for future reference.

- When you are confident that the circuit is working properly and that you understand its behavior, schedule a post-lab meeting with me at a mutually agreed time before the deadline posted on the Laboratory page at the course web site. The following guidelines apply:

    - Read these guidelines and the "Post-Lab Meeting" section below **well in advance of the meeting.**
    - All group members must be present.
    - The meeting will take place in the Maker-E if Dana 307 is not available at the scheduled time.
    - Meetings will be scheduled in the order that requests are received. The order might be determined by random assignment. Meetings will not be scheduled during a lecture, lab, or recitation section for another course. Please notify me of time conflicts.
    - Meetings will not be rescheduled if the first one reveals circuit problems, wiring failures, errors in the test procedure, or a lack of preparation.
    - Deadline extensions will generally be approved for confirmed illnesses or other extenuating circumstances.
    - Meetings may take place before the end of the lab session if other groups do not need assistance. You do not have to remain in the lab room after the meeting ends.

Post-Lab Meeting

At the beginning of the post-lab meeting, your group must demonstrate that both biasing circuits are operating properly. Your group may choose a spokesperson to present the demonstration, or you may involve everyone. The demonstration must:

- Report all resistor values used in each circuit. If a potentiometer is used for R_1 in the two-resistor bias circuit, then its effective value must be measured during the demonstration.
- Show that the value of V_C in the four-resistor circuit is close to the specified value.
- Show that the value of V_C in the two-resistor circuit is close to the specified value.
- Show how the collector voltage in each circuit changes when heat is applied.

Next, each group member will be asked to respond to a randomly selected prompt from the numbered list on the next page and possibly answer a few follow-up questions. Note that:

- Each group member must answer a different prompt.
- Each person will have a time limit of **seven minutes** in which to respond.
- Responses must be supported by high-quality visual aids, including a properly labeled diagram (or diagrams).
- Factors that could negatively affect the individual score include excessive delays during the response, inability to answer questions without hints or prompting (e.g., if responses seem to be rehearsed without comprehension), excessive delays in setting up demonstrations, and lack of preparation.

You should organize the physical circuit layouts so that group members can switch between demonstrations quickly.

A tentative list of discussion prompts is given below. More prompts could be added, or one of those below could be replaced or modified. Any changes will be announced in advance.

1. Explain how you verified that the BJT's power rating was not exceeded in each circuit.
2. Explain the process used to determine the values of R_1 and R_2 in the four-resistor bias network. Include any important design decisions.
3. Explain the process used to adjust the value of R_1 in the two-resistor bias network to meet the specifications.
4. Explain why the two-resistor circuit exhibits so much instability relative to the four-resistor circuit. (The response must be more detailed than just "There is no negative feedback," or a similar response. Explain what happens when the temperature changes.)
5. Explain qualitatively how the four-resistor bias network responds to variations in the β value of the BJT and therefore maintains stable bias conditions.
6. Explain qualitatively or quantitatively why the value of I_2 (the current through R_2) in the four-resistor network should be 10 or more times the base current to obtain stable bias conditions.

Lab Scoring Criteria

Each group member will receive a score based on the following criteria quantized at the indicated levels. The first three criteria constitute a group base score; that is, each group member will receive the same score for those three criteria. The remaining criterion will be assessed independently and will be determined by that person's contribution to the post-lab meeting. The rubrics posted on the Laboratory page at the course web site will guide the assignment of the various scores.

0, 8, 15, 23, 30 pts	Functional 4-resistor bias circuit with reasonable resistor values (group)
0, 8, 15, 23, 30 pts	Functional 2-resistor bias circuit with reasonable resistor values (group)
0, 2, 5, 8, 10 pts	Quality and effectiveness of supporting visual aids (group)
0, 8, 15, 23, 30 pts	Quality of response to prompt (indiv.)

If the meeting is completed after the deadline, a 10-pt score reduction will be applied for every 24 hours or portion thereof that it is late (not including weekend days) unless extenuating circumstance apply. No credit for the individual criterion will be given four or more days after the deadline. Up to 60 pts will be assigned to each member of the group for the first two criteria if at least one group member demonstrates functional circuits within a week of the deadline.

Group Assignments

The randomly generated groups for this lab exercise are listed below:

Jiorle- Ren-Sagoe
Andrews- Powick-Samuels
Beebe-Piper-Tuncel-Youn