Lab #2: Emitter Follower Amplifier Design

Introduction

A wide range of amplifier topologies are available that are well suited for specific types of applications. A common-collector BJT amplifier, more commonly called an *emitter follower*, is often used when high output current and very low output impedance are required. Impedances of just a few ohms to tens of ohms can be achieved by setting the quiescent collector current to an appropriate value. In this lab exercise you will design and assemble an emitter follower circuit with an output impedance of 50 Ω and then verify via measurements whether the circuit meets specifications. Lab groups are listed at the end of this handout.

Theoretical Background

The classic emitter follower circuit topology is shown in Figure 1. Because the output signal is taken from the emitter terminal, it is not necessary to develop a signal voltage swing at the collector, so a collector resistor is not needed. The collector voltage can be at signal ground potential. As in the other amplifier circuits we have studied, the DC blocking capacitors C_i and C_o are made large enough so that their reactances are negligible at the lowest frequency of interest.

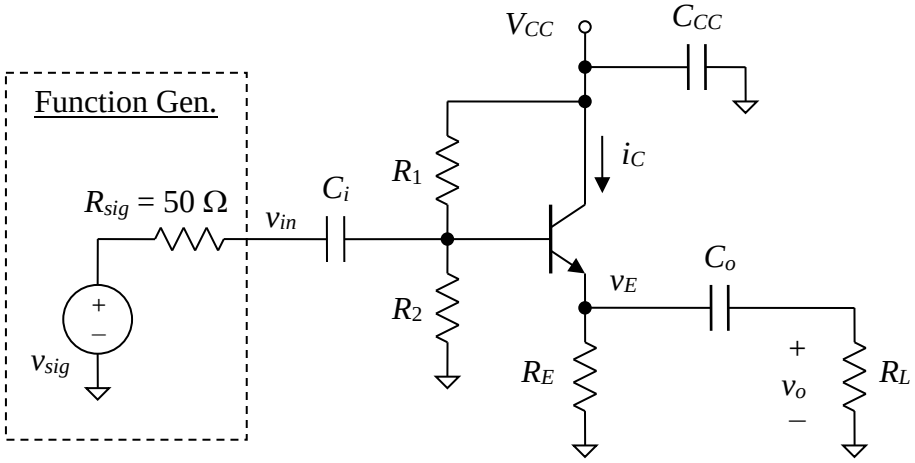

Figure 1. Emitter follower circuit using an *npn* BJT. The Thévenin equivalent circuit consisting of v_{sig} and R_{sig} represents the bench-top function generator.

The small-signal behavior of the circuit can be analyzed using either the hybrid-pi model or the T model of the BJT. Both models are shown in Figure 2. The small-signal transconductance g_m used in both models is given by

$$g_m = \frac{I_C}{\eta V_T},$$

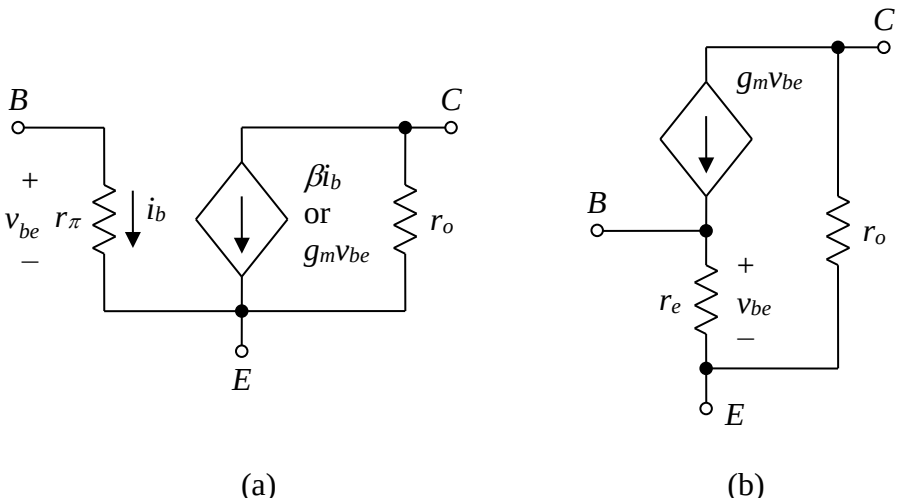

Figure 2. (a) The hybrid-pi model and (b) the T model of the BJT for small-signal analysis. These models are valid at relatively low operating frequencies (below 1 MHz or so). The terminals labeled *B*, *C*, and *E* represent the base, collector, and emitter terminals, respectively. Resistance r_o is often omitted to simplify analyses.

where I_C is the quiescent collector current, η is the emission coefficient for the *pn* junction ($\eta = 1$ is usually assumed), and V_T is the thermal voltage (roughly 25 mV at room temperature). Several equivalent expressions relate the value of resistance r_e in the T model to the other parameters:

$$r_e = \frac{\eta V_T}{I_E} = \frac{\alpha \eta V_T}{I_C} = \frac{\alpha}{g_m} = \frac{r_\pi}{\beta + 1},$$

where $I_C = \alpha I_E$ (equivalently, $\alpha = \beta/(\beta + 1)$) and resistance r_π in the hybrid-pi model is given by

$$r_\pi = \frac{\eta V_T}{I_B} = \frac{\beta \eta V_T}{I_C} = \frac{\beta}{g_m}.$$

Experimental Procedure

- Design an emitter follower like the one shown in Figure 1 using a 2N3904 *npn* BJT (data sheet is available at the course web site) with the following specifications:
    - power supply voltage $V_{CC} = 12$ V
    - small-signal output resistance $R_{out} \approx 50\ \Omega$ (±20 Ω)
    - quiescent emitter voltage $V_E \approx 6$ V (±1 V)
    - no-load ($R_L \rightarrow \infty$) voltage gain $v_o/v_{in} > 0.95$ for 400 Hz to several tens of kHz
    - negligible phase shift from input to output for load resistances as low as 40 Ω (*Hint*: This requires careful selection of the values of C_i and C_o)
    - base biasing resistor values that represent a reasonable compromise between bias stability, current demand from the power supply, and high input resistance
    - value of C_{CC} not critical; use 10, 22, or 47 μF for good performance at audio frequencies

You will have to select appropriate bias current levels, resistor values, and some capacitor values to meet the specifications. Assume a reasonable value for the emission coefficient η and the thermal voltage V_T. Guidance on r_o and β values is available via the datasheet; you might need to consult the notes on h-parameters available at the course Moodle site.

Verification Opportunity: If your group requests it, I will check the expression for the output resistance that you derive and help you work through any corrections if necessary. The request will be honored only if you have a legible and well-organized description of the derivation and only if you have at least read Important Note #1 below. The description may be handwritten. Verifications may take place within or outside of the lab sessions. You may also simulate your circuit using *Multisim* to verify your design, but this is not required.

Important Note #1: Remember that the small-signal output resistance depends on the values of g_m and R_E (and perhaps other quantities). There is interaction between g_m and R_E because both values are related to the quiescent collector current, so at first it might appear that the values of g_m and R_E have to be determined simultaneously using a set of complicated coupled equations. However, remember that in many cases only one quantity will have a dominant effect on the output resistance. Consider the typical values for g_m and R_E. If you make use of that knowledge, the design process simplifies considerably, but be sure to verify any assumptions that you make after the design is completed.

Important Note #2: The capacitor values should be chosen so that the voltage drops across them are negligible at 400 Hz or higher. In the case of C_o, remember that R_L varies and can have a value as low as 40 Ω. Avoid values for C_i and C_o that are excessively large. It is not always necessary to make the capacitive reactance just a few ohms or less. Its reactance only needs to be low enough so that the voltage drop across it has a negligible effect on the voltage gain. Consider the estimated input and output resistances of the amplifier. Be sure to orient electrolytic capacitors properly (i.e, watch the polarity); the orientation should be based on the expected *total* voltage across the capacitor.

Important Note #3: Keep a high-quality record of your design process for future reference, especially for the post-lab discussion. It should include an explanation of how you selected all component values as well as power dissipation analyses. A written description will not have to be submitted, but all lab group members should understand the details.

- Assemble the emitter follower circuit on a protoboard, and devise a set of tests to verify that the circuit is meeting all specifications (R_{out}, V_E, and open-circuit voltage gain). Start by checking that the DC bias levels are correct. Verify that the amplifier is producing the appropriate output voltage for various load resistances and that the BJT is not entering the cut-off or saturation regions (or operating nonlinearly) for reasonably small input signal voltages.

  Important Note #4: You can apply an input voltage of a few tens of mVpk or more if R_L is relatively large because of the significant negative feedback introduced by the combined resistance ($R_E||R_L$). However, if R_L is relatively small (around 50 Ω or less), then the input voltage should be kept below about 5–10 mVpk (or maybe less) to maintain linearity. Be able to explain why the small-signal condition varies with the value of R_L.

Important Note #5: When power is applied to the amplifier, the total load voltage might initially have a large DC offset voltage that drifts in value over time, with longer settling times associated with larger values of R_L (especially if it is hundreds of kilohms or more). The DC component of the load voltage should settle to zero eventually. Make sure that you understand why this happens.

Important Note #6: Consider carefully how to measure the value of R_{out} (output resistance). The test procedure cannot involve the application of an external test source at the output port as is done with pencil-and-paper analysis or might be done in *Multisim*. Doing so risks damaging the circuit or the signal generator, and it can be difficult to measure the test current, which is a signal current. (We do not really have the equipment to do that.) The open circuit/short circuit method should not be used either. Applying a short across the output terminal of an amplifier (especially a high-power one) is not a good idea! Again, we have no reliable way to measure the signal current. In short, methods that are fine for paper analysis are not necessarily advisable for a real circuit. Instead, consider measuring the signal voltage across two different R_L values. Think carefully about what their values should be to obtain accurate results.

Important Note #7: If the measured value of R_{out} differs from the target value by only 20 to 50%, then it is possible that the assumed value for the emission coefficient η differs significantly from the actual value. You may redesign the circuit for a different η value if you wish. A discrepancy in the value of R_{out} that is greater than 50% or so most likely indicates a wiring or design error or an incorrectly chosen output capacitor value.

- Compile the following data and visual aids so that you can easily refer to them during your post-lab meeting. The items may be handwritten or drawn, but they must be legible and well organized with no extraneous notes or information. Figures, tables, captions, and equations must be formatted according to the guidelines posted on the Laboratory page at the course web site.

    - Brief explanation of the output resistance measurement procedure with sufficient supporting visual aids and equations but minimal text; minimize "visual clutter"
    - Measured value of R_{out}
    - Description of redesign for new emission coefficient η value (if applicable)
    - Complete circuit diagram with component values clearly indicated, including polarities of electrolytic capacitors
    - Additional supporting diagrams and/or equations if needed
    - Any observations or troublesome issues noted during the experiment

  Combine all of the visual aids that your group intends to use into a single PDF document and **e-mail** it to me before the post-lab meeting begins. The file name should have the form:

  "LName1_LName2_LName3_Lab2_sp24.pdf"

  Add "LName4" if your group has four members. **The file size must be less than 5 MB.** Keep a copy if you wish to use it to prepare for the next exam or need it for future reference.

- Schedule a post-lab meeting (length up to 30 min) with me at a mutually agreed time before the deadline posted on the Laboratory page at the course web site. The purpose is to assess each group member's comprehension of the design process, measurements, and observations of circuit performance. The meeting could cover any aspect of the design and related topics. The following guidelines apply:

    - Read these guidelines and the "Post-Lab Meeting" section below well in advance of the meeting.
    - All group members must be present.
    - The meeting will take place in the Maker-E if Dana 307 is not available at the scheduled time.
    - Meetings will be scheduled in the order that requests are received. The order might be determined by random assignment. Meetings will not be scheduled during a lecture, lab, or recitation section for another course. Please notify me of time conflicts.
    - Meetings will not be rescheduled if the first one reveals circuit problems, wiring failures, errors in the test procedure, or a lack of preparation.
    - Deadline extensions will generally be approved for confirmed illnesses or other extenuating circumstances.
    - Meetings may take place before the end of a lab session if other groups do not need assistance. You do not have to remain in the lab room after the meeting ends.

Post-Lab Meeting

At the beginning of the post-lab meeting, we will review your design process and verify and discuss the items listed below. Your group may choose a spokesperson for this portion, or you may involve everyone.

- Specified quiescent emitter voltage V_E
- Design process used to obtain reasonable values for C_i and C_o
- Design process used to set the value of R_{out} (output resistance)

Next, each group member will be asked to respond to one of the prompts from the numbered list on the next page and possibly answer a few follow-up questions. Note that:

- Each person will have a time limit of **five minutes** in which to respond.
- You may assign the prompts to group members before the meeting.
- Each response must be supported by high-quality visual aids prepared by the respondent, including a properly labeled circuit diagram (or diagrams).
- The physical circuit layout and connections to equipment should be organized so that group members can switch between demonstrations quickly.
- Visual aids must be complete enough for understanding but not so excessive that they create visual clutter that detracts from clarity.
- Figures, tables, captions, and equations must be formatted according to the guidelines posted on the Laboratory page at the course web site.
- Factors that could negatively affect the individual score include excessive delays during the response, inability to answer questions without hints or prompting (e.g., if responses seem to be rehearsed without comprehension), excessive delays in setting up demonstrations, lack of preparation, and of course any missing required items.

A likely list of discussion prompts is given below. More prompts could be added, or one of those below could be replaced or modified. Any changes will be announced in advance. Assign the fourth prompt only if your group has four members.

1. Explain the procedure used to measure the value of R_{out}, and apply the procedure to your emitter follower circuit to show that the measured value is close to the specified value.
2. Use the oscilloscope to simultaneously display the input and output voltage waveforms for the R_L = 47 kΩ case (approximates an open circuit). Verify that the amplifier operates linearly and that the correct voltage gain is depicted. Explain why the gain remains fairly constant as long as the value of R_L is above roughly 500 Ω.
3. Use the oscilloscope to simultaneously display the input and output voltage waveforms for the $R_L \approx 50\ \Omega$ case. Verify that the amplifier operates linearly and that the correct voltage gain is depicted. Explain why distortion occurs at much lower input voltage magnitudes in this case than in the no-load ($R_L \to \infty$) or large-R_L case.
4. **[for 4-person groups only:]** Explain why the measured output voltage waveform for large values of R_L initially has a significant DC offset voltage that eventually decays. Also explain the factor(s) that determines the rate of decay.

Lab Scoring Criteria

Each group member will receive a score based on the following criteria quantized at the indicated levels. The first two criteria constitute a group base score; that is, each group member will receive the same score for those criteria. The remaining criteria will be assessed independently and will be determined by that person's contribution to the post-lab meeting. The rubric posted on the Laboratory page at the course web site will guide the assignment of scores.

0, 8, 15, 23, 30 pts	Functional circuit w/appropriate component values (group)
0, 8, 15, 23, 30 pts	Effectiveness of procedure for measuring R_{out} (group)
0, 2, 5, 8, 10 pts	Quality and effectiveness of supporting visual aids (indiv.)
0, 8, 15, 23, 30 pts	Quality of response to prompt (indiv.)

If the meeting is completed after the deadline, a 10-pt score reduction will be applied for every 24 hours or portion thereof that it is late (not including weekend days) unless extenuating circumstance apply. No credit for the individual criteria will be given four or more days after the deadline; however, up to 60 pts will be assigned to each member of the group for the first two (group) criteria if at least one group member demonstrates a functional circuit and an effective measurement procedure within a week of the deadline.

Group Assignments

The randomly generated groups for this lab exercise are listed below:

Beebe-Youn-Piper
Powick-Jiorle-Samuels
Sagoe-Andrews-Ren-Tuncel