Lab #3: BJT Current Mirror and Differential Amplifier

Introduction

Differential amplifiers ("diff amps") constitute an important class of amplifier circuits. They are widely used as the first stage in many op-amp ICs, in data transmission systems (like Ethernet and USB), and in specialized signal processing circuits. The differential amplifier produces an output signal that is proportional to the difference between two input voltages, but it can be used as a single-ended amplifier as well. Even in the latter role, it has advantages over more traditional amplifier configurations, including stable biasing using a small number of resistors, no need for large bypass capacitors within the circuit, and good frequency response characteristics. In this lab exercise you will design, assemble, and test a BJT-based differential amplifier biased by a simple current mirror to meet a set of specifications. Lab group assignments are listed at the end of this handout.

Theoretical Background

A basic diff amp circuit is shown in Figure 1. A current mirror (Q_A and Q_B) is used to generate a bias current I_{EE} for the two amplifying transistors Q_1 and Q_2. If Q_1 and Q_2 and the two collector resistors R_C are identical and if the quiescent base voltages of Q_1 and Q_2 are equal, then the bias current splits evenly between the two BJTs; thus, the circuit shown in Figure 1 would truly be practical only in an integrated circuit implementation.

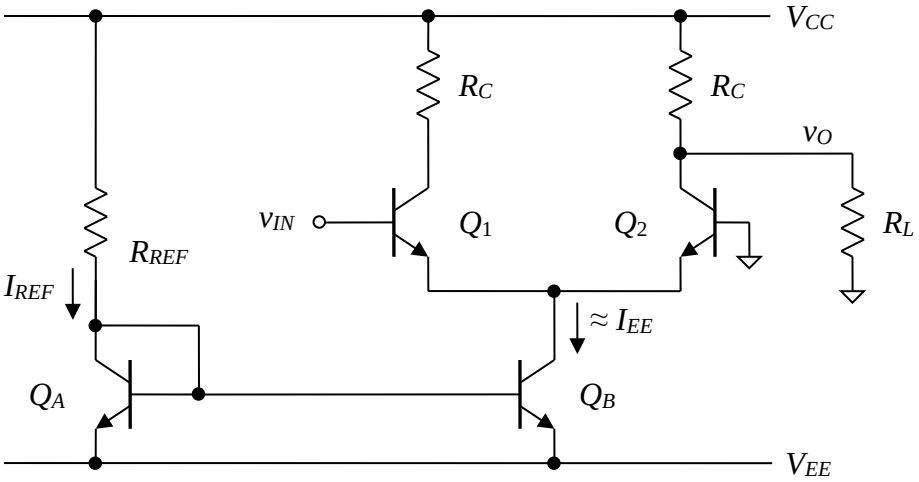

Figure 1. Single-ended differential amplifier with resistor loads and biasing via a simple current mirror.

The amplifier considered here takes a single-ended input voltage v_{IN} and produces a single-ended output voltage v_O. A *single-ended* voltage is one that is defined relative to ground. Compare this to a *differential* voltage that is defined between two floating (ungrounded) nodes. The term *single-ended* likely has come about because that type of voltage can be represented in a

schematic diagram using a single circle (a "single end") with a voltage label next to it, like "v_{IN}" in Figure 1. Note that v_{IN} and v_O as labeled in Figure 1 are *total* voltages. The quiescent bias voltage applied to the base of Q_1 is normally, but not always, zero. In this lab exercise, it will be zero because you will be driving the amplifier with the bench-top function generator with zero average output voltage.

Experimental Procedure for Lab Session #1

- Design and assemble a simple BJT current mirror like the one shown in Figure 1 using a CA3046 *npn* transistor array IC to meet the following specifications:
    - Nominal output current I_{EE} near compliance limit: 500 μA
    - Bipolar power supply (V_{CC} and V_{EE}): ±5 V
    - Resistor R_{REF}: standard 5% value closest to calculated value
    - Recommendation: Use Q3 and Q4 in the CA3046 diagram for the mirror circuit. Q1 and Q2, which are a matched pair, should be reserved for the diff amp section. Q5 should be avoided because it is connected to the chip's substrate and therefore is not well matched to the other BJTs.

- Verify that the current mirror is producing close to the desired value of I_{EE} by loading it with a series of resistors ranging from roughly 1 kΩ to 20 kΩ. (The test resistor replaces the diff amp circuitry in Figure 1 between V_{CC} and the collector of Q_B.) To obtain a useful data set that clearly illustrates the mirror's behavior, you should use at least 12 test resistors – 15 to 20 would be better. The value of I_{EE} will vary from the intended value, especially for smaller test resistances. (Do you know why?)

- Assume that the mirror circuit can be represented by a Norton equivalent circuit consisting of current source I_{EE} and resistance R_{EE} as shown in Figure 2. Record a wide range of values of the load current I_L as you vary the resistance R_{test}. Consult the notes on the next page as guidance for these measurements. Using *Excel* or *Matlab*, prepare a professional-quality plot of I_L vs. R_{test} based on your measured data. Include a descriptive title, label the axes, and include appropriate units. Use the plot to identify the compliance voltage, and use your measured data to determine the Norton equivalent circuit of the current mirror. Keep good records of your current mirror test procedure and the results, because you will have to briefly explain your procedure and present the calculated value of I_{EE} and R_{EE} at the beginning of the second lab session. **The plot must be submitted by the date specified at the course Laboratory web page, which is before the second lab session.**

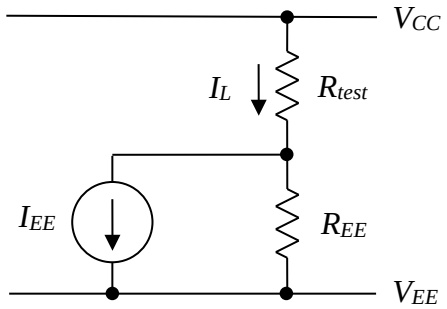

Figure 2. Current mirror test circuit with mirror represented by a Norton equivalent circuit. Resistor R_{test} replaces the diff amp circuitry in Figure 1.

Requirements, Recommendations, and Advice for Current Mirror Tests:

Take an extensive enough range of data to produce a well-defined curve and to identify the load conditions for which the mirror no longer operates properly. Use the appropriate range of your measured data to determine the Norton equivalent circuit of the current mirror (i.e., the values of I_{EE} and R_{EE}). Note that I_{EE} is not simply equal to the measured current at one of the data points, and it cannot be assumed to be equal to the specified value of 500 μA. Its value, like the value of R_{EE}, must be determined from your measured data. Keep good records, because you will have to explain your procedure and present the calculated values of I_{EE} and R_{EE} during the post-lab meeting.

You cannot use information from the CA3046 or LM3046 datasheet to determine R_{EE} because your test conditions are different from those used to obtain the data quoted in the datasheet. Moreover, there are wide variations in the properties of individual transistors. The plots and tables in the datasheet describe only typical behavior. It is highly unlikely that the value of I_{EE} in your circuit will be exactly equal to the datasheet value. Both I_{EE} and R_{EE} must be determined using your measured data.

Finding good values for I_{EE} and R_{EE} requires good measurements. If your data are noisy and/or your plot is not relatively linear for the case when both BJTs are in the active region, then your calculated values for I_{EE} and R_{EE} are likely to be incorrect. Double-check your test circuit for errors, and consider using a linear interpolation method on your measured data.

The datasheet for the CA3046 is available at the ECEG 351 Laboratory web site. You might discover that you can find a value for the transistor output resistance r_o from the datasheet. It is related to the old h-parameter h_{oe}. However, as stated above, remember that the plots and tables in the datasheet describe only typical behavior and might not be fully relevant to your circuit. The datasheet can provide only ballpark figures, not actual values for a given device.

<u>Experimental Procedure for Lab Sessions #2 and #3</u>

- Early in the second lab session, your group must present a brief demonstration that includes the elements listed below. The time limit is 10 minutes, so make sure that your circuit is operating reliably and that all of your presentation materials are accessible. Preparation will factor heavily into the assigned score. The information may be presented by any number of members of the lab group, but all group members must be present. The order of demonstrations will be determined randomly, and the first one will begin at 10:10 am.

    1. Confirm that your current mirror circuit is operating properly (i.e., $I_L \approx I_{EE}$) with a load resistance of 10 kΩ.
    2. Present a professional-quality plot of I_L vs. R_{test}.
    3. Use the plot to estimate the compliance voltage of the mirror circuit.
    4. Explain how you used the plot and/or measured data to determine the Norton equivalent circuit of the current mirror. Your explanation must be supported by one or more clear and legible figures and equations. Figures, tables, and equations must be formatted following the guidelines posted on the Laboratory page at the course web site.

- When you are not demonstrating your current mirror circuit, design a diff amp circuit with a single-ended input and output like the one shown in Figure 1 using a CA3046 *npn* transistor array IC to meet the following specifications:

    - Minimum single-ended small-signal voltage gain magnitude (with load): 50 V/V
    - Minimum voltage gain must be available down to DC (0 Hz)
    - Load resistance range: 100 kΩ to 1 MΩ
    - Output voltage swing above and below quiescent point: at least ±0.5 V
    - Minimum single-ended input resistance: 2 kΩ
    - Bipolar power supply (V_{CC} and V_{EE}): ±5 V
    - Nominal mirror current (I_{EE}): 500 μA

    The signal source will be the bench-top function generator. Its default quiescent output voltage is 0 V, and its output resistance is 50 Ω.

    READ THE FOLLOWING IMPORTANT NOTES! THEY WILL SAVE YOU TIME AND FRUSTRATION.

    Important Note #1: Read Note 1 on p. 2 of the CA3046 data sheet. If you do not heed the warning, your circuit probably will not work properly.

    Important Note #2: Two of the BJTs on the IC are closely matched and are intended for use as a differential pair; consult the data sheet. Pay very close attention to the maximum ratings, such as maximum power dissipation per transistor and maximum collector-emitter voltage. You might need to account for the transistor Early resistance r_o in your design. It is related to the old h-parameter h_{oe}.

    Important Note #3: Select reasonable component values that satisfy the specifications yet do not exceed the various device ratings and other practical limits. Observe the common-mode range of the diff amp (i.e., keep Q_1 and Q_2 within the active region). Some specifications might be very easy to meet, and some might require some thought. There is likely to be considerable variation between the various lab groups' designs. *Hint*: The quiescent output voltage V_O in this circuit is directly related to the small-signal voltage gain. It might be helpful to derive the relationship before you proceed with your design.

    Important Note #4: The load resistance R_L will upset the amplifier's symmetry to some degree, but careful design choices can minimize the effect. Consider using a Thévenin equivalent circuit to represent the V_{CC}-R_C-R_L combination as seen by the collector of Q_2 for quiescent (bias) analysis purposes.

    Important Note #5: To suppress noise and prevent oscillations, connect bypass capacitors between the power supply leads (the V_{CC} and V_{EE} nodes) and ground. A value of 10 μF is about right. Keep these connections relatively short and near the IC, and pay attention to the capacitors' polarities. The capacitor values should be large enough so that the reactances are no more than a few tens of ohms at a few hundred hertz. Additional capacitors of 0.1 μF or so in parallel with the larger bypass capacitors might further mitigate any problems with noise and/or oscillations, especially in the MHz range. The smaller capacitors should be closer to the IC than the larger ones.

Important Note #6: A printed circuit board for the diff amp circuit might be available by lab session #2. It will most likely be populated with all of the components except the collector resistors, load resistors, and reference resistors, which will be added via on-board terminal blocks. You will be notified if and when the PC board becomes available.

- Keep a detailed record of the design choices that you make. In particular, be able to explain your choices for the values of R_C and any trade-offs that you considered between the gain and quiescent collector voltage.

- Assemble the diff amp circuit, and verify that the quiescent collector voltages are close to the design value (some variation is to be expected, possibly up to a volt). Record your measurements; you will need them later.

- Verify by measurement that the diff amp is providing the specified minimum voltage gain. Keep in mind that the input signal voltage needs to be very small because the amplifier has substantial gain and is easily driven to the point of clipping. Furthermore, recall that this type of amplifier suffers from nonlinearity if the peak input voltage is more than 0.5 to 1 times the quantity ηV_T (i.e., more than 20–25 mV or so at room temperature). If the positive half-cycle and negative half-cycle of the output waveform do not have the same magnitudes, then the amplifier is probably operating nonlinearly. If that is the case, then you should attach an attenuator to the output of the function generator or build one of your own. Any attenuator that you use or build should maintain the function generator's output resistance of 50 Ω. Eliminate as much noise as possible from the screen image, and use the manual cursors to measure voltage levels; noise makes automatic measurements unreliable.

- Capture oscilloscope screen images of the input and output voltage waveforms being simultaneously displayed for the R_L = 100 kΩ and 1 MΩ cases, and add to them a summary of the single-ended voltage gain calculations from your measurements. The screen captures will be referred to during the post-lab meeting.

- Compile the following material for reference during the post-lab meeting. All items should be legible and well organized. Figures, tables, captions, and equations must be formatted according to the guidelines posted on the Laboratory page at the course web site.

    - Diagram of amplifier circuit with component values and key voltages and currents clearly indicated
    - Brief outline of the current mirror test procedure and results
    - Plot of load current vs. test resistance taken during current mirror tests and mirror output resistance calculation
    - Key aspects of the design process for the amplifier
    - Quiescent collector voltage measurements for Q_1 and Q_2 with and without a load
    - Annotated oscilloscope screen captures showing input and output voltage waveforms for linear operation for R_L = 100 kΩ and 1 MΩ

  Combine all of the items above into a single PDF document and **e-mail** it to me before the post-lab meeting begins. The file name format should have the form:

  "LName1_LName2_LName3_Lab3_sp24.pdf"

Add "LName4" if your group has four members. **The file size must be less than 5 MB.** Keep a copy if you wish to use it to prepare for the next exam or need it for future reference.

- Schedule a post-lab meeting (length up to 30 min) with me at a mutually agreed time before the deadline posted on the Laboratory page at the course web site. The purpose is to assess each group member's comprehension of the design process, measurements, and observations of circuit performance. The meeting could cover any aspect of the design and related topics. The following guidelines apply:

    - Read these guidelines and the "Post-Lab Meeting" section below well in advance of the meeting.
    - All group members must be present.
    - The meeting will take place in the Maker-E if Dana 307 is not available at the scheduled time.
    - Meetings will be scheduled in the order that requests are received. The order might be determined by random assignment. Meetings will not be scheduled during a lecture, lab, or recitation section for another course. Please notify me of time conflicts.
    - Meetings will not be rescheduled if the first one reveals circuit problems, wiring failures, errors in the test procedure, or a lack of preparation.
    - Deadline extensions will generally be approved for confirmed illnesses or other extenuating circumstances.
    - Meetings may take place before the end of a lab session if other groups do not need assistance. You do not have to remain in the lab room after the meeting ends.

Post-Lab Meeting

Each group member will be asked to respond to one of the prompts from the numbered list starting below and possibly answer a few follow-up questions. The following guidelines apply:

- Each person will have a time limit of **five minutes** in which to respond.
- You may assign the prompts to group members before the meeting.
- Each response must be supported by high-quality visual aids prepared by the respondent, including a properly labeled circuit diagram (or diagrams).
- The physical circuit layout and connections to equipment should be organized so that group members can switch between demonstrations quickly.
- Visual aids must be complete enough for understanding but not so information-packed that they are overwhelming or create visual clutter that detracts from clarity.
- Figures, tables, captions, and equations must be formatted according to the guidelines posted on the Laboratory page at the course web site.

The prompts are listed below:

1. Explain how you selected the collector resistor values for your design. In particular, explain how you incorporated the ±0.5 V output voltage swing specification and how you ensured that the BJTs remain in the active region over a complete sinusoidal cycle.

2. Show that both no-load (i.e., $R_L \rightarrow \infty$) quiescent collector voltages are close to the specified value, and demonstrate and explain the change that occurs when a 100 kΩ load is added. That is, explain why one or both of the quiescent collector voltages changes. (The mismatch between the BJTs is not the primary cause.)
3. Use the oscilloscope to simultaneously display the total input and output voltage waveforms for the R_L = 100 kΩ and R_L = 1.0 MΩ cases. Verify linear operation for both cases, and use the measured waveforms to verify that the voltage gain exceeds the specified minimum value. Explain why the gain differs for the two cases.
4. **[for 4-person groups only:]** Explain how your group ensured during the design process that the differential input resistance would be at least 2 kΩ.

Lab Scoring Criteria

Each group member will receive a score based on the following criteria quantized at the indicated levels. The first two criteria constitute a group base score; that is, each group member will receive the same score for those criteria. The remaining criteria will be assessed independently and will be determined by that person's contribution to the post-lab meeting. The rubrics posted on the Laboratory page at the course web site will guide the assignment of scores.

0, 8, 15, 23, 30 pts	Functional mirror circuit w/proper NEC & compliance values (group)
0, 8, 15, 23, 30 pts	Functional diff amp circuit w/appropriate component values (group)
0, 2, 5, 8, 10 pts	Quality and effectiveness of supporting visual aids (indiv.)
0, 8, 15, 23, 30 pts	Quality of response to prompt (indiv.)

If the meeting is completed after the deadline, a 10% score deduction will be applied for every 24 hours or portion thereof that it is late (not including weekend days) unless extenuating circumstance apply. No credit for the individual criteria will be given four or more days after the deadline; however, up to 60 pts will be assigned to each member of the group for the first two (group) criteria if at least one group member demonstrates a functional mirror circuit and diff amp within a week of the deadline.

Group Assignments

The randomly generated groups for this lab exercise are listed below:

Beebe-Powick-Ren
Andrews-Piper-Samuels
Jiorle-Sagoe-Tuncel-Youn