Lab #10: Emitter Follower with Specified Frequency Response

Introduction

Emitter follower circuits are frequently employed in applications that require an amplifier or cascade of amplifiers with a very low output impedance. An example is shown in Figure 1. The circuit has been biased so that the emitter resistance \( r_e \) is approximately 50 \( \Omega \). Recall that the output impedance of an emitter follower is close to \( r_e \) if the source impedance \( R_{sig} \) is not too large. The open-circuit voltage gain is very close to unity, but it rolls off at frequencies above and below its mid-band range of operation. In this lab exercise you will design an emitter follower circuit to have a specified frequency range and then verify via measurements that the circuit meets specifications. Lab groups are listed at the end of this handout.

![Figure 1. BJT-based emitter follower. The Thévenin equivalent circuit consisting of \( v_{sig} \) and \( R_{sig} \) represents the bench-top function generator. Resistors \( R_1 \), \( R_2 \), and \( R_E \) have been selected to establish a stable quiescent collector current of 500 \( \mu \)A.](image)

Experimental Procedure

You must arrive at the lab session by 10:00 am, although an earlier arrival is recommended to avoid running out of time due to unanticipated problems. The instructor will be in the lab room 8:00-11:00 am. Demonstrations will be observed on a first-come, first-served basis. Complete the following steps:

- Specify the capacitors in the emitter follower circuit shown in Figure 1 so that the low-frequency cut-off is 300 Hz (the low end of the human voice range). Use the smallest possible capacitor values to satisfy the design requirement. The pole frequencies should be separated by a factor of ten so that only one is dominant. Provide a clear, well organized, and
legible record of your design process as part of the lab summary. It should include symbolic
expressions for each pole frequency and descriptions of how they were obtained. In the case
of the power supply bypass capacitor $C_{CC}$, provide a justification for the value you select.

- Assemble the emitter follower circuit using a 2N3904 npn BJT. A data sheet is available at
the course web site. Confirm that the quiescent current and voltage levels are correct to verify
partially that the circuit is working properly. Also confirm that the mid-band gain is correct
and that the BJT is not entering the cut-off or saturation regions. Note that the mid-band gain
under load is nowhere close to unity. This is as it should be. (Why?)

- Now determine the frequency response of the circuit and plot it over a logarithmic frequency
scale. A complete set of data consists of the voltage gain magnitude in dB vs. frequency and
the phase shift vs. frequency. Take sufficient data over a wide enough frequency range so
that the roll-off is clearly evident and so that it is clear that the mid-band gain extends well
above the cut-off frequency. Do not print out the plot yet.

- After you are satisfied that your circuit is working properly, demonstrate it to the instructor.
This should include a quick scan across the frequency range of interest.

- The internal capacitances $C_\pi$ and $C_\mu$ of the BJT introduce a high-frequency roll-off that starts
well above the audio frequency range. However, the upper cut-off frequency can be lowered
by adding a discrete capacitor to the circuit. Select a location and value for an additional
capacitor that will set the upper cut-off frequency to 6 kHz. Include a record of your design
process in your lab summary.

- Take another set of frequency response measurements to verify that the high-frequency roll-
off occurs as specified and that the lower cut-off frequency is still close to 300 Hz. You may
now print out the frequency response plot. Identify the cut-off frequencies on the plot,
compare them to the specified values, and comment on the results. Be sure to record any
additional relevant data such as the tolerances of the capacitors and resistors.

- After you are satisfied that the modified circuit is working properly, demonstrate it to the
instructor. This should include another quick scan across the frequency range of interest.

Lab Summary

After your group has completed the design task and demonstrated a properly working circuit,
compile the following items into a single document:

- Record of design process.
- Properly annotated plots of the gain in dB and phase shift in degrees vs. frequency (log
scale), including descriptive titles or captions and indications on the magnitude plot of the
upper and lower cut-off frequencies that mark the limits of the mid-band range.
- Interpretation of results and discussion of implications and observations. The ideas presented
here should be original and focus on outcomes that are new, not quite what was expected, or
at least not obvious.
The summary is due in class on Wednesday, April 10, 2013. One summary per group should be submitted and may be handwritten on notebook paper. Summaries will not be graded directly for writing issues, but they must be legible and understandable.

**Grading**

Each group member will receive the same grade based on the following criteria. Scores for the three lab summary items will be quantized at the 0, 2, 5, 8, and 10-point levels.

- 30% Properly assembled circuit
- 40% Demonstration of properly operating circuit
- 10% each Bulleted items listed in the “Lab Summary” section above

As outlined in the lab policies and guidelines, any group member who misses any portion of the lab session and is not excused will receive a grade penalty proportional to the time absent.

Lab summaries submitted after the deadline but before 5 pm on the following Thursday will have a 20% grade deduction applied. No credit will be given for a summary submitted later, although credit for successful assembly and demonstration (70% maximum) will still be given.

If the demonstration is not completed by the end of the lab session but is completed by 5:00 pm that day, a 10% grade deduction will be applied. If the demonstration is completed by 4:00 pm the following day, a 20% grade deduction will be applied. No demonstration credit will be given thereafter.

**Group Assignments**

The randomly generated groups for this lab exercise are listed below:

- Selvaggio-Hoolachan
- Wetzel-Selevan
- DeMelis-Collins
- Reisser-Levine
- Fast-Hecht
- Dost-Donatelli
- Swaim-Chhean-Abels

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